WIDEBAND DYNAMIC BIASING OF POWER AMPLIFIERS FOR WIRELESS HANDHELD APPLICATIONS

A Thesis
Presented to
The Academic Faculty

by

Jau-Horng Chen

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2006

WIDEBAND DYNAMIC BIASING POWER AMPLIFIERS FOR WIRELESS HANDHELD APPLICATIONS

Approved by:

Dr. J. Stevenson Kenney, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Thomas G. Habetler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. W. Marshall Leach, Jr.
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Vinu Govind
Jacket Micro Devices Inc.

Dr. Gabriel A. Rincon-Mora
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: June 30, 2006

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

AC	Alternating Current
ACLR	Adjacent Channel Leakage power Ratio
ACPR	Adjacent Channel Power Ratio
AM	Amplitude Modulation
AMPS	Advanced Mobile Phone Service
BW	Bandwidth
CDMA	Code Division Multiple Access
CFR	Crest Factor Reduction
CLCC	Ceramic Leadless Chip Carrier
CMOS	Complementary Metal-Oxide-Semiconductor
CORDIC	Codinate Rotational Digital Computer
DC	Direct Current
EDGE	Enhanced Data rates for GSM Evolution
EER	Envelope Elimination and Restoration
EF	Envelope Following
ET	Envelope Tracking
FET	Field Effect Transistors
FM	Frequency Modulation
GMSK	Gaussian Minimum Shift Keying
GPRS	General Packet Radio Service
GSM	Global System for Mobile Communication
HPSK	Hybrid Phase Shift Keying
IC	Integrated Circuit
LHP	Left Half Plane
LINC	Linear Amplification with Nonlinear Components
MMIC	Microwave Monolithic Integrated Circuit
NADC	North American Digital Cellular
OQPSK	Offset Quadrature Phase Shift Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PT	Power-level Tracking
PAR	Peak-to-Average Ratio
PM	Phase Modulation
PWM	Pulse Width Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave
SMD	Surface Mount Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network

SUMMARY

The objective of the proposed research is to extend the battery life in cellular handsets by improving the transmitter efficiency. Bandwidth efficient modulation formats, such as W-CDMA, encode much of the information in amplitude modulation. Therefore, linear transmitters must be used so as not to increase transmission errors, and cause interference in adjacent bands. Various engineering trade-offs were examined to find a suitable transmitter architecture for W-CDMA. Dynamic biasing of the transmitter power amplifier (PA) provides a simple way to improve efficiency for applications that require highly linear amplification. The envelope elimination and restoration (EER) PA or EER-based polar-modulated PA is an attractive solution since it has potential to achieve very high efficiency with high linearity. However, the major impediment to EER implementation has been the lack of power-efficient dynamic power supply circuits that can operate with sufficient modulation bandwidth, and simultaneously achieve the required modulation linearity. This work proposes several solutions to this problem.

First, a dynamic supply circuit using delta modulation was designed and implemented. An open-loop EER PA with 48% peak efficiency was constructed and tested with a cellular band IS-95 CDMA signal with a bandwidth of 1.25 MHz. The low switching loss by using a delta modulator made the implementation of a wideband dynamic biasing circuit possible.

Second, a dynamic supply circuit using dual-phase PWM was designed and implemented to achieve wider bandwidth, lower noise, and higher efficiency. An open-loop EER PA was implemented with the dynamic supply IC. A digital gain compensation

scheme was developed to further increase bandwidth and linearity. This enables a dynamic supply circuit with lower switching frequency to have larger usable bandwidth with little increased power consumption. A cellular band W-CDMA voice signal was used to evaluate the performance of the overall PA. The PA achieved 50% efficiency while passing all required spectral specifications of W-CDMA standard. To increase the inherent low dynamic range of an EER PA, a dual-mode power amplifier combining an EER PA and power-level tracking PA was proposed. The dual-mode PA is the first W-CDMA PA to improve both average efficiency and peak efficiency while covering the whole W-CDMA dynamic range.

This work will contribute to the development of high efficiency, small-sized multi-mode linear PAs for battery-operated wireless handheld devices.

CHAPTER 1

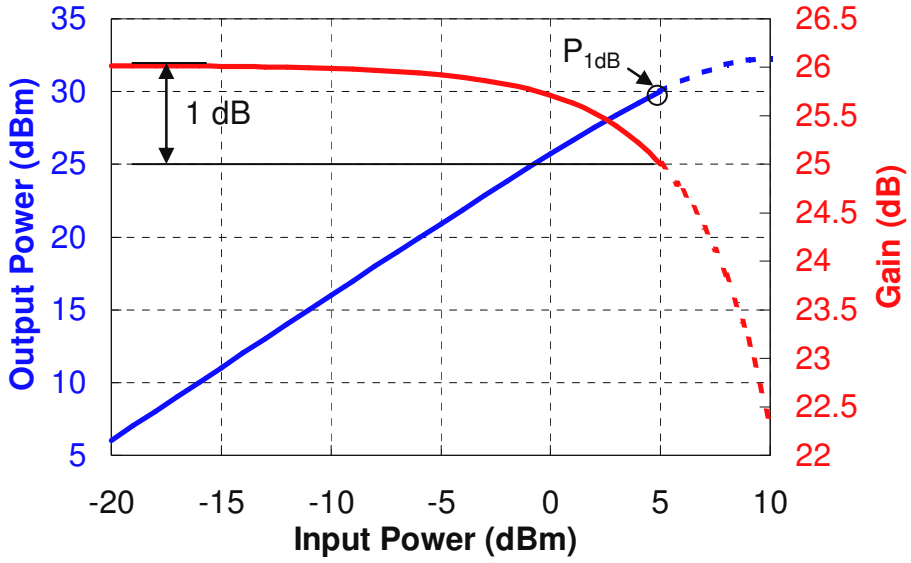
INTRODUCTION

Wireless handheld devices have gained significant popularity over the past three decades since the introduction of the first cellular phone in the 1970s. Over the years, the advance of semiconductor technology has led to substantial size reduction of wireless handheld devices. However, the improvement of battery technology has been limited throughout these years. The battery is a major limitation for the size, weight, and operational time of a wireless handheld device. Since major breakthroughs for increasing the battery capacity do not appear to be on the horizon, reducing the overall power consumption is the only viable solution for longer battery life.

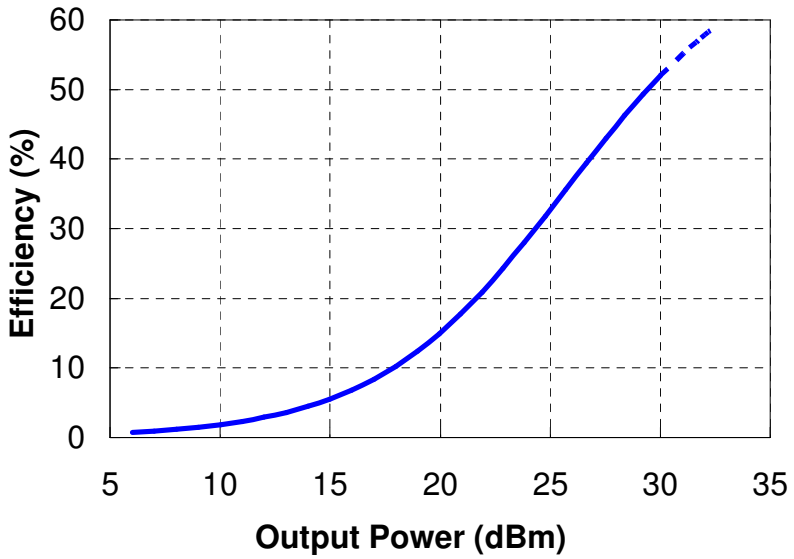
The power amplifier (PA) accounts for a signification portion of the overall power consumption in a wireless handheld device. Improving the efficiency of the PA can greatly reduce the overall power consumption of the RF front-end and thus increase the battery life [1]. Today, most wireless applications use complex modulation schemes with a non-constant envelope to achieve greater spectral efficiency. This makes efficient and linear power amplification crucial in wireless handheld devices. Conventional PAs operating in class-A/B mode have significantly lower efficiency when backed-off from the peak output power level. In addition, to maintain a specific linearity requirement, the PA can not operate too close to the compression point. This leads to the need for using larger power transistor size and increases the cost of the overall RF front-end. The following sections discuss several wireless standards and the previous methods that have been proposed to improve the efficiency of the PA.

1.1 Wireless Standards and Modulation Schemes

PAs are more efficient when highly overdriven or saturated. Simulation result of a typical PA is shown in Figure 1.1. The PA shows efficiency over 50% beyond the 1 dB compression point; however, the efficiency drops quickly once the PA is backed-off from peak power. Applications that use modulation schemes with constant envelope, such as the conventional analog frequency modulation (FM) used in Advanced Mobile Phone Service (AMPS) and Gaussian minimum shift keying (GMSK) used in the Global System for Mobile Communication (GSM) standard, can utilize saturated power amplifiers to achieve high efficiency. To achieve higher spectral efficiency, more and more wireless standards adopt modulation schemes with non-constant envelope such as NADC, EDGE, IS-95 CDMA, W-CDMA, IEEE STD 802.11 WLAN, and IEEE STD 802.16 WiMax. Power amplifiers for these applications have to operate in the less efficient linear region and also have to be backed-off by the peak-to-average ratio (PAR), which further reduce the efficiency. Battery life of portable devices for these applications is usually significantly lower than that of devices using saturated power amplifiers. However, with low quiescent current in class-AB PAs and careful power control between the handheld device and basestation the power consumption can be somewhat reduced.



(a) Gain



(b) Efficeincy

Figure 1.1 Typical gain and efficiency of a conventional PA.

To limit interference in some applications, power control is utilized to ensure that the basestation receives equal power from each mobile device. In IS-95 and W-CDMA, the power amplifier actually operates around 5 dBm more often, instead of the peak power. Since linear PAs are usually biased in class-AB, power control reduces the quiescent current while reducing the output power level, which improves efficiency. However, the battery life of IS-95 and W-CDMA cellular handsets are still shorter than GSM handsets, as is seen in the following analysis. The probability distribution function of RF PA output power for reverse-link IS-95 is shown in Figure 1.2 as reported from two different research groups [3–5]. The average RF output power is defined as

$$\overline{P}_{out} = \int P_{out}\, p(P_{out})\, dP_{out}, \tag{1.1}$$

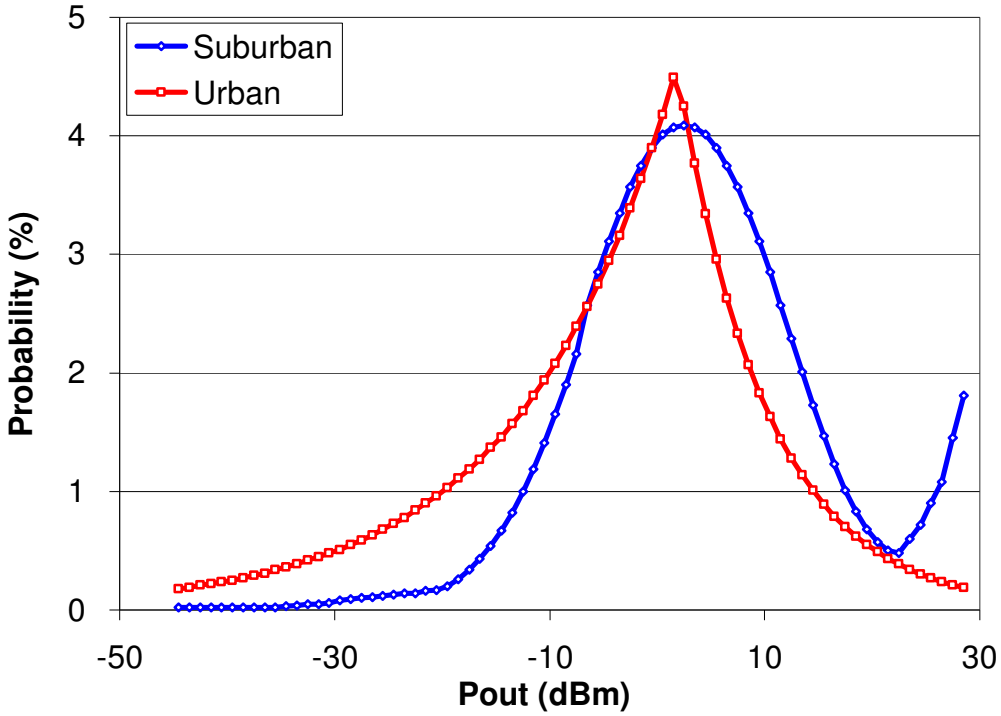
and the average DC power consumption is defined as

$$\overline{P}_{dc} = \int P_{dc}(P_{out})\, p(P_{out})\, dP_{out}, \tag{1.2}$$

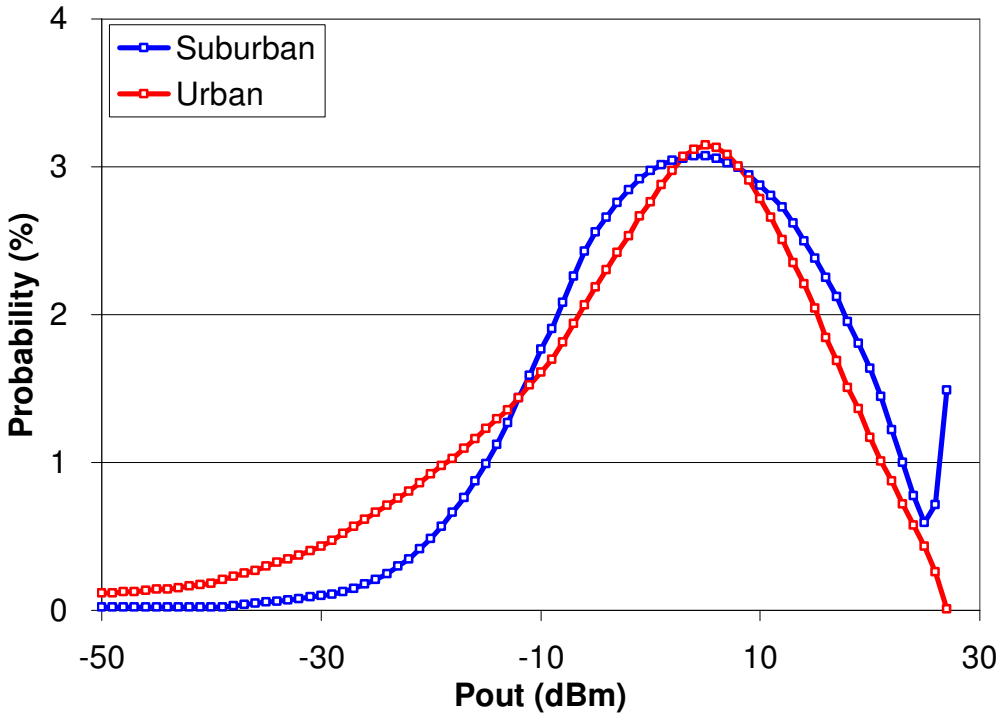
The average efficiency can be determined by

$$\overline{\eta}_d = \frac{\overline{P}_{out}}{\overline{P}_{dc}} = \frac{\int P_{out}\, p(P_{out})\, dP_{out}}{\int P_{dc}(P_{out})\, p(P_{out})\, dP_{out}}, \tag{1.3}$$

where P_{out} is the output power level, $p(P_{out})$ is the probability of an output power level P_{out}, and $P_{dc}(P_{out})$ is the DC power consumption at an output power level of P_{out}. To achieve maximum overall efficiency, the PA efficiency should be optimized where $P_{dc}(P_{out})p(P_{out})$ is high. Modulation schemes and power control range (PCR) specifications for various wireless standards are summarized in Table 1.1 [6–9].



(a) Probability distribution function reported in [3]



(b) Probability distribution function reported in [4, 5]

Figure 1.2 Probability distribution function of IS-95 CDMA PA output power.

Table 1.1 Summary of wireless standards

Standard	PAR (dB)	Modulation	PCR (dB)	Channel BW
AMPS	0	Analog FM	None	30 kHz
NADC	3.5	π/4-QPSK	35	30 kHz
GSM	0	GMSK	30	200 kHz
IS-95 CDMA	5.1	OQPSK	80	1.25 MHz
EDGE	3.2	8PSK	30	200 kHz
W-CDMA	3.34 ~ over 10	HPSK	80	5 MHz
WLAN	10	Adaptive	None	20 MHz
WiMax	12	Adaptive	50	1.5~20 MHz

1.2 Power Amplifier Efficiency Enhancement Schemes

To improve the efficiency of a linear PA, efficiency enhancement schemes such as predistortion, Doherty, outphasing, and dynamic biasing are usually used [1]. The following sections describe the basic operation of the aforementioned methods and discuss the pros and cons of each method.

1.2.1 Predistortion

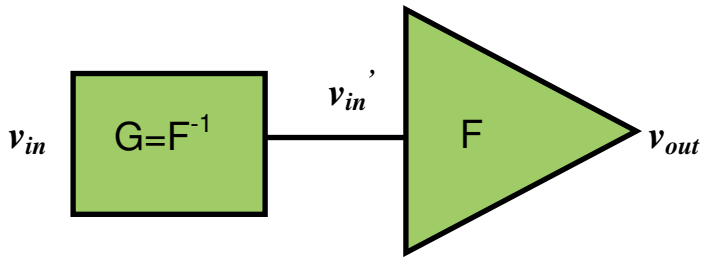
A PA is usually linear at low power levels. As the power level increases, the PA becomes more nonlinear and the gain of the PA compresses. Assume the PA gain can be expressed as a nonlinear function of the input signal,

$$v_{out} = F(v_{in}) = \sum_{n=1}^{\infty} a_n v_{in}^n . \tag{1.4}$$

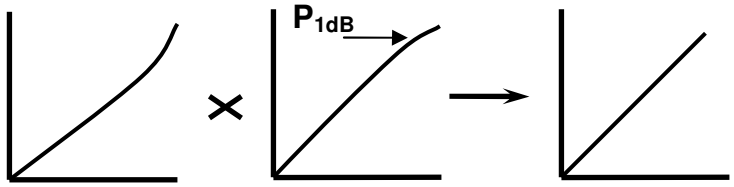
A function G can be found, such that

$$v_{out} = F(G(v_{in})) = kv_{in}, \tag{1.5}$$

where k is a constant. This suggests by first preconditioning the input signal, the overall amplification is linear. Such preconditioning is called predistortion [52]. The basic block diagram of an open-loop predistortion system is shown in Figure 1.3.



(a) Block diagram



(b) Basic operation

Figure 1.3 Block diagram of an open-loop predistortion system and its operation.

With predistortion, the power amplifier can be operated close to or even beyond the compression point. This allows the peak power to be increased, resulting in improved efficiency and higher output power. This also means to achieve the same output power level, smaller, less expensive RF power transistors can be used with predistortion. Such measures can reduce the size of the heat sink and the overall cost. Currently, implementations of predistortion systems have been limited to basestation applications. The main reason has been the required additional circuitry for implementing the inverse function that significantly increases the size, cost, and complexity of the overall predistorted PA. The additional computation of the inverse function and adaptation of

inverse function also consume too much power that may lead to degraded efficiency for handheld applications.

1.2.2 Doherty

The Doherty technique uses a high-power main PA and a low-power auxiliary PA in parallel. The block diagram of a Doherty PA is shown in Figure 1.4. The main PA is usually biased in Class-B region, while the auxiliary PA is biased in Class-C region. For low power levels, only the main PA is used; the input power is not able to turn on the auxiliary PA. For high power levels where the main PA saturates, the auxiliary PA turns on to maintain an overall linear output. To have the auxiliary PA match the gain compression characteristics of the main PA is difficult since the input bias of the two amplifiers must be carefully controlled. Therefore, to overcome the problem, predistortion is sometimes used [13]. Another issue is the size of the λ/4 transformers. For current wireless handheld devices, operating frequencies are usually around 1 or 2 GHz. Implementing λ/4 transformers on board with micorstrip transmission lines will be about 2 cm to 4 cm in length and is not attractive for handheld devices. While smaller lumped element equivalent circuits may be used, they can significantly impact the peaking amplifier efficiency. For this reason, Doherty PAs have also been relegated to base stations.

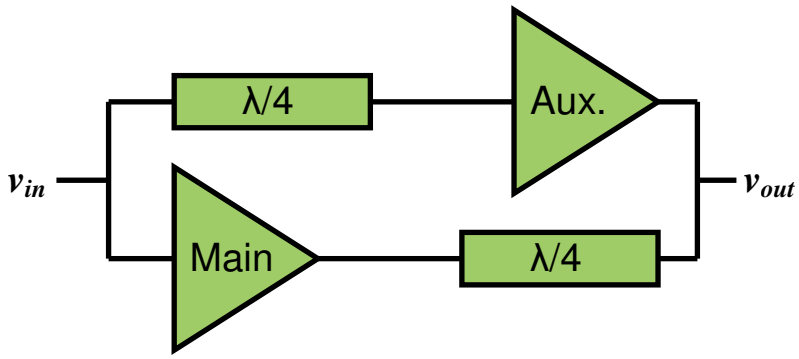


Figure 1.4 Block diagram of a Doherty PA.

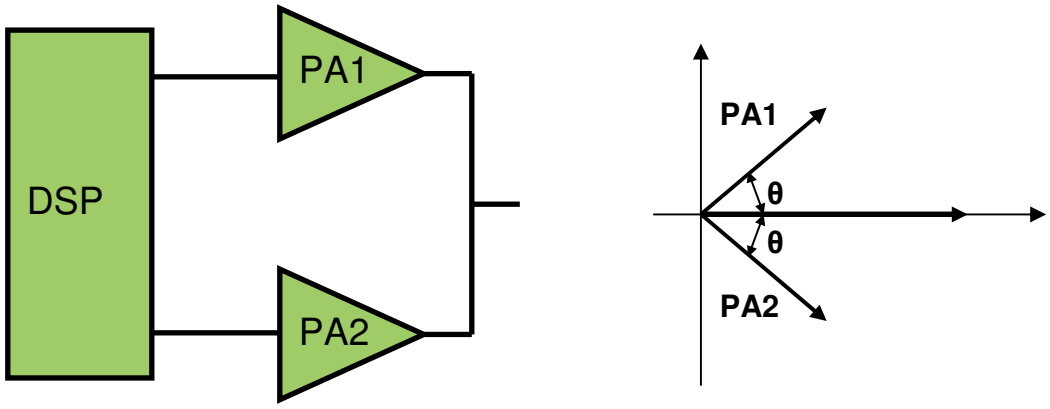
1.2.3 Outphasing Technique

The outphasing technique uses two identical PAs in parallel [15]. By changing the phase difference between the two PAs the output amplitude can be changed. Assuming the phase difference between the two PAs is 2θ, the signal of the two PAs can be written as $A_m\cos(\omega_c t+\theta)$ and $A_m\cos(\omega_c t-\theta)$, where A_m is the signal amplitude and ω_c is the carrier frequency. The combined signal of the two PAs can be written as

$$output = 2A_m \cos(2\theta)\cos(\omega_c t)\,. \tag{1.6}$$

The output signal amplitude is a function of, 2θ, the phase difference. Since the output signal amplitude is not a function of the input amplitude, the two PAs can be power-efficient saturated PAs.

Matching between the two PAs is a main limitation for implementing the outphasing technique. Assume the amplitude mismatch between the two PAs is ΔA_m, the peak output is $2A_m+\Delta A_m$. For large amplitudes, a small ΔA_m causes few problems. However, for modulation schemes with zero-crossing, the two phases can not fully cancel and the overall output amplitude is ΔA_m. The result of the mismatch is similar to clipping the signal and may degrade overall linearity.



(a) Block diagram (b) Basic operation

Figure 1.5 Block diagram and basic operation of an outphasing PA.

1.2.4 Dynamic Biasing

Dynamically biasing of the power amplifier is an attractive way to improve the power amplifier efficiency since less direct current (DC) power is needed when the output power level is low. Compared to predistortion where an additional receiver chain is required, Doherty method and outphasing technique where additional large transmission line circuits are needed, dynamic biasing has less complexity and hence lower cost. PAs utilizing Doherty or outphasing techniques may also require additional predistortion to meet linearity requirement as in [14, 15], while the additional power loss does not justify the increased cost for handheld applications. Dynamic biasing of the PA provides a low power, low distortion, and cost effective solution for improving PA efficiency.

The envelope elimination and restoration (EER) technique is a form of such dynamic biasing PA. It is able to achieve high-efficiency, linear power amplification by using a highly nonlinear, but efficient, power amplifier with drain or collector voltage modulated by an efficient switching power supply circuit [2]. Since the power amplifier

can operate as a switch, the efficiency can be high. Because of the difficulties in implementing an EER PA such as implementing high-efficiency wideband supply circuits and generating constant envelope driving signals, various simplified versions of the EER PA such as envelope tracking (ET) PA and envelope following (EF) PA have been investigated throughout the years since the invention of the EER PA in the 1950's. One such version is power-level tracking (PT) PA, which tracks only the slow-varying average power level, instead of the fast-varying envelope, and modulates the drain or collector voltage of a linear PA. Among the aforementioned methods, the dynamic biasing technique has the lowest cost and is the easiest to implement. Currently, the power tracking technique is the only efficiency enhancement scheme used in commercial wireless handheld devices.

This work identifies the trade-offs in the design of an EER PA to optimize the overall system efficiency. A delta modulated supply circuit and a dual-phase PWM supply circuit were proposed to implement the wideband supply circuit in an EER PA. Using additional digital signal processing with little computational power such as crest factor reduction (CFR) and digital gain compensation in conjunction with the dynamic supply circuit, EER PA for wideband applications with bandwidths of several MHz can be implemented with efficiency over 50%, while previous implementations have bandwidths limited to a few hundreds of kHz [17-19].

1.3 Outline of Thesis

The thesis is organized as follows. Chapter 2 compares different ways to bias a PA for improved efficiency. In addition, different system architectures of dynamic biasing PAs and transmitters are summarized and compared.

Chapter 3 shows the development of an open-loop EER PA using a delta-modulated dynamic supply circuit. Design and implementation of a 150 MHz dynamic supply circuit using delta-modulation is presented. Subsequently, the measurement setup and measurement results using a cellular band IS-95 CDMA signal are shown.

Chapter 4 demonstrates a dual-phase PWM dynamic supply circuit and its application to an open-loop EER PA for W-CDMA applications. System level requirements are first simulated and summarized. Modeling of the RF PA and measurement setup are then discussed. The next section shows the development of digital envelope path gain compensation for increasing the bandwidth and linearity of an EER PA. Development of crest factor reduction for polar modulated signals is discussed in 4.7. Section 4.9 demonstrates a dual-mode PA combining a conventional EER PA for high power levels and PT PA for low power levels to increase the inherent low dynamic range of conventional EER PAs.

Finally, the thesis is concluded in Chapter 5 with a summary of the work covered and key contributions of the work.

CHAPTER 2

DYNAMIC BIASING OF POWER AMPLIFIERS

2.1 Introduction

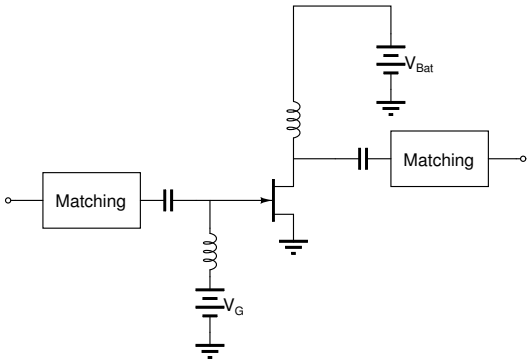
A power amplifier may not always operate at the peak output power level. For wireless standards that use non-constant envelope modulation schemes or PA power control, the PA is more likely to be operated in back-off. Since the RF output power is reduced, it is desirable to reduce the DC power consumption to increase efficiency under back-off. This chapter discusses various ways to bias a power transistor and the trade-offs associated with each technique.

2.2 Biasing of Power Amplifiers for Improved Efficiency

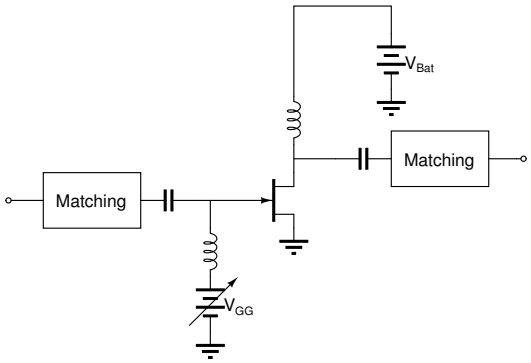
Cost, efficiency, and distortion are the main concerns in selecting the bias scheme for a PA. Four bias schemes shown in Figure 2.1 are discussed in this section. PAs using field effect transistors (FET) are being considered here, but all bias schemes may also be applied to PAs using bipolar transistors.

2.2.1 Power Amplifiers with Fixed Biasing

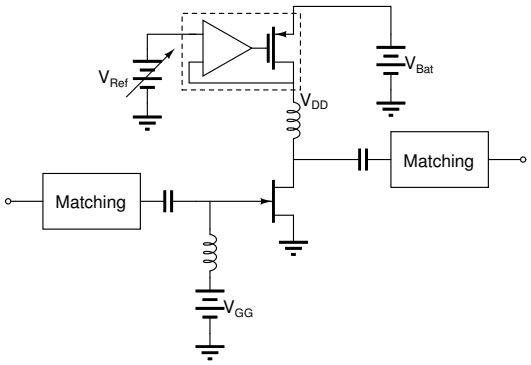
The most common way to bias a PA is fixed biasing, where both the gate and the drain voltages are constant, as shown in Figure 2.1(a). The gate is connected to a fixed voltage that defines the quiescent current, and the drain is connected to the battery through an RF choke. The amplifier is usually biased in class-A/B mode with a relatively small conduction angle to reduce the quiescent current and conserve power.



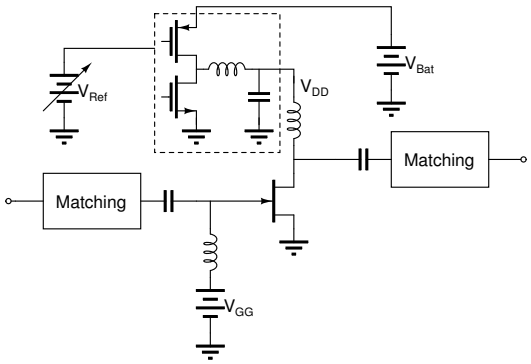
(a) Fixed biasing



(b) Dynamic biasing of gate



(c) Dynamic biasing of drain using linear regulator



(d) Dynamic biasing of drain using switching regulator

Figure 2.1 Biasing of power amplifiers.

2.2.2 Dynamic Biasing of Gate

The gate voltage defines the quiescent current of the power amplifier. By reducing the gate voltage closer to the threshold voltage, the quiescent current reduces and so does the conduction angle. Under power back-off conditions, reducing the gate voltage can increase the efficiency. The configuration of a PA utilizing dynamic biasing of the gate is shown in Figure 2.1(b). Changing the gate voltage can alter the behavior of a PA considerably. The change of AM/PM and AM/AM characteristics is shown in [10]. The change is significant as the gate voltage approaches the threshold voltage. Another issue is that any change at the gate of the power amplifier will be amplified; thus noise

becomes an important issue when modulating the gate voltage. The major benefit of this configuration is its relatively small size. Since the dynamic biasing circuit does not need to pass through all of the output power, the size of the circuit can be small and can be integrated into the PA MMIC as in [11].

2.2.3 Dynamic Biasing of Drain Using Linear Regulators

Changing the drain voltage changes the load line of a power amplifier. By reducing the drain voltage of a PA, the RF signal can traverse a larger portion of the load line, which leads to higher efficiency. The AM/PM and AM/AM characteristics of PAs utilizing dynamic biasing of drain and gate are compared in [10]. The amplitude distortion and phase distortion are lower when the drain is dynamically biased instead of the gate. For PAs using dynamic biasing of the drain, almost all of the current that flows through the PA must flow through the dynamic biasing circuit. This leads to a large-sized pass transistor in the linear regulator, as shown in Figure 2.1(c), which needs to be capable of handling current in excess of 2 Amperes as in GSM applications with negligible drop-out voltage. At peak output power level, any drop-out voltage will directly reduce the maximum output power of the PA. The efficiency of the linear regulator can be approximated as

$$\eta_{LR} = \frac{V_{DD}}{V_{BAT}}. \tag{2.1}$$

To the linear regulator, the PA can be modeled as a load with a resistor in parallel to a DC current source, as shown in Figure 2.2. When the PA is biased closer to the class-A region, the PA resembles a DC current source. However, the PA load is closer to a resistor when it is operating near saturation. When the PA is closer to a DC current

source, reducing the drain voltage with a linear regulator does not increase the efficiency since the DC power consumption remains fairly constant. The overall efficiency can be written as

$$\eta = \eta_{LR}\eta_{PA} = \frac{V_{DD}}{V_{BAT}}\frac{P_{out}}{V_{DD}I_{load}} \approx \frac{P_{out}}{V_{BAT}I_{DC}}, \tag{2.2}$$

which is the same as the efficiency of a PA with fixed biasing. In GSM and other applications that use saturated PAs, the PA resembles more of a resistor and the DC power consumption can be written as

$$P_{dc} = V_{BAT}I_{load} \approx \frac{V_{BAT}V_{DD}}{R_{DS}}, \tag{2.3}$$

As the supply voltage of the PA, V_{DD}, is reduced, the DC power consumption is reduced approximately by the same factor. Such a reduction in DC power consumption leads to higher efficiency than PAs with fixed biasing under backed-off conditions.

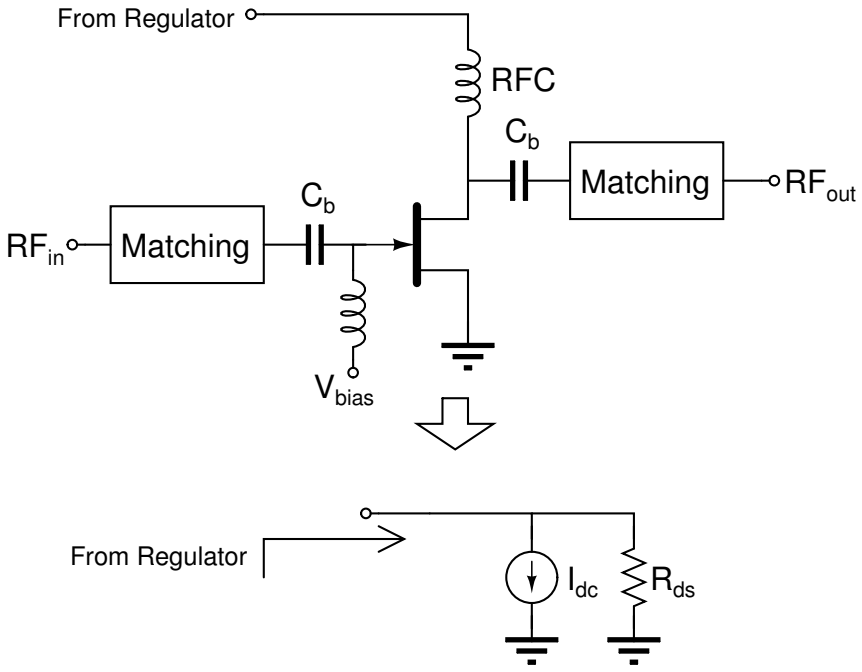


Figure 2.2 PA as a load to the regulator.

2.2.4 Dynamic Biasing of Drain Using Switching Regulators

When the PA is backed-off from peak output power, the linear regulator becomes lossy. By using a buck switching regulator instead of a linear regulator, as shown in Figure 2.1(d), efficiency can be greatly increased at voltage levels considerably lower than the battery voltage. At peak output power, the switching regulator suffers from the same problem in the linear regulator, where the regulator itself has DC loss. The maximum output voltage of the switching regulator is

$$V_{out,\max} = V_{BAT} - I_{load}(R_{DS,on} + DCR), \tag{2.4}$$

where I_{load} is the load current, $R_{DS,on}$ is the on resistance of the power transistor, and DCR is the DC resistance of the inductor. To achieve the same voltage drop as in a linear regulator, the transistor size has to be larger to reduce $R_{DS,on}$ and an inductor with lower DC resistance has to be used. Such an inductor is usually larger in size. The large power transistor size usually leads to a large die size and higher cost, while the large-sized inductor takes up too much board space and may have problems fitting in a handheld device. Dynamic biasing of the drain using a switching regulator has the best performance among all four biasing schemes, but its use has been limited because of cost issues.

2.3 Power Amplifiers and Transmitter Architectures Using Dynamic Biasing

Linear power amplification with high efficiency is highly desirable for today's wireless applications. Cascaded power-hungry linear power amplifiers have been widely used for wideband linear applications such as WLAN and W-CDMA. To increase battery life in handheld devices, the Doherty technique, Chirex out-phasing method, and dynamic

biasing techniques have been the main focus of linear PA efficiency enhancement in recent years. Demonstrations of the Doherty technique for handheld applications are shown in [12–14]. A major problem in implementing this technique is the need for λ/4 transformers for impedance transformation. For W-CDMA and IEEE 802.11b/g WLAN, the λ/4 transmission lines will be around 2 cm, which takes up too much board space for handheld devices. In the Chirex method, or linear amplification with nonlinear components (LINC), a combiner is required to combine two out-phased signals from two PAs. The main difficulty is the need for a low-loss combiner at the output of the PA since any loss there directly reduces the overall efficiency. The implementation of the Chirex method for 802.11a has been shown in [15]. Dynamically biasing the gate or drain of a PA is more attractive than the previous two methods since the additional bias circuitry is easier to integrate with lower cost. The following is a review and comparison of various linear PAs or transmitter architectures employing the dynamic biasing schemes.

2.3.1 Envelope Elimination and Restoration

A typical complex-modulated RF signal can be written as

$$I(t)\cos(\omega_c t) + Q(t)\sin(\omega_c t) = Env(t)\cos(\omega_c t + \phi(t)), \tag{2.5}$$

where

$$Env(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{2.6}$$

is the envelope information,

$$\phi(t) = \tan^{-1}\frac{Q(t)}{I(t)} \tag{2.7}$$

is the phase information, and ω_c is the carrier frequency. For an EER PA, the phase information and envelope information are extracted from the original modulated signal

and processed separately. The phase information is used to drive the gate or base of the PA transistor. Since the phase information has a constant envelope, the PA can be highly overdriven to achieve high efficiency. The envelope information is fed into the dynamic power supply circuit so the supply voltage of the PA will change accordingly. By changing the supply voltage, the output waveform will be shaped and the overall amplification can be linear [2]. The basic block diagram of an EER PA is shown in Figure 2.3.

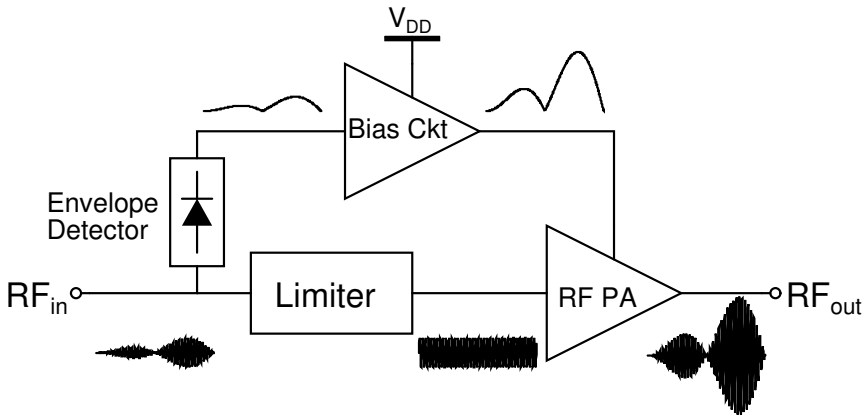


Figure 2.3 Block diagram of a basic EER PA.

The use of the EER technique for basestation applications is shown in [16, 17] and for handset applications in [18, 19]. Its use has been limited to narrowband applications because of the limited bandwidth in conventional switching power supply circuits. Current commercial switching power supply circuits usually have a switching frequency of less than 2 MHz, with a bandwidth of only a small fraction of the switching frequency. For wireless standards such as IS-95, UMTS, and 802.11, the RF channel bandwidth is higher than the switching frequency of most commercially available switching power supply circuits. The envelope signal, as shown in (2.6), is a nonlinear

transformation of the original I(t) and Q(t) signals and has a wider bandwidth than the original RF signal [20]. A power-efficient power supply circuit with a bandwidth higher than the envelope signal of today's wireless applications is highly desirable for implementing an EER PA [21].

The RF PA in an EER PA is not an ideal multiplier such that the output envelope signal can be distorted. The time delay difference between the envelope path and the phase path can also deteriorate the combined signal. Envelope feedback was used in [17–19] to reduce distortion and delay difference. For wideband applications, the limited bandwidth in the envelope detectors can also be a problem in implementing an EER PA.

2.3.2 Envelope Tracking

The envelope tracking (ET) technique is a simplification of the EER technique [9, 22, 23]. Instead of extracting both the phase information and the envelope information, only the envelope information is extracted. The RF PA is operated in the linear region and its supply voltage changed according to the envelope information. The supply voltage is varied with sufficient headroom to minimize distortion. With the headroom provided, the implementation of an ET PA is easier than an EER PA since delay matching is not as crucial as in EER PA. The block diagram and operation of an ET PA are shown in Figure 2.4.

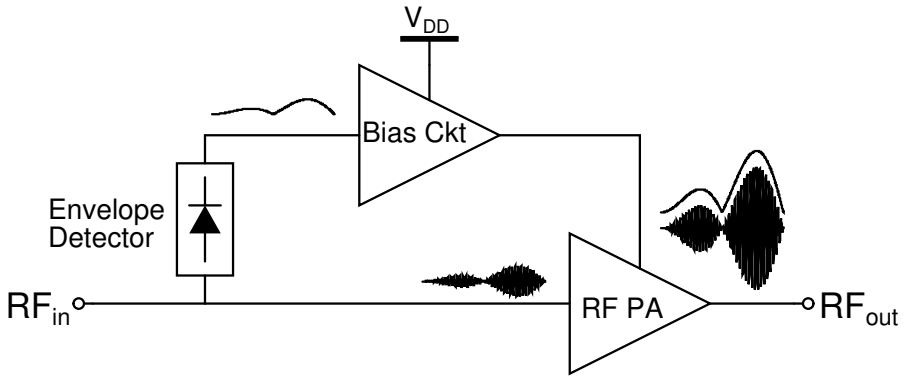


Figure 2.4 Block diagram of an ET PA.

The major drawback in an ET PA is its lower efficiency because of operating the RF PA in the linear region. Operating with sufficient headroom also reduces the power output capability of the PA. In an ET PA, the gain of the RF PA reduces as the supply voltage decreases. For high peak-to-average signals and applications that require large power control range, the gain variation is a source of nonlinearity. An additional gate dynamic biasing circuit was used in [22] and pre-distortion was used in [9] to reduce such effect. As with the EER technique, the ET PA needs a dynamic power supply circuit with a bandwidth wider than the bandwidth of the envelope signal. For wideband applications, the lack of an efficient dynamic power supply circuit is the main problem for implementation.

2.3.3 Envelope Following

The envelope following (EF) technique is similar to the envelope tracking technique in that the RF modulated signal does not need to be decomposed. The input and output signals can be written as

$$v_{in}(t) = Env_{in} \cos(\omega_c t + \phi_{in}(t)) \tag{2.8}$$

and

$$v_{out}(t) = Env_{out} \cos(\omega_c t + \phi_{out}(t)) . \tag{2.9}$$

Linear amplification requires

$$\frac{Env_{out}(t)}{Env_{in}(t)} = G \tag{2.10}$$

and

$$\phi_{out}(t) = \phi_{in}(t) + \phi_{offset} , \tag{2.11}$$

where G, the system gain, and ϕ_{offset} are constant [24]. The system gain can be held constant by using envelope feedback. A PA with low phase distortion is needed since there is no feedback loop for phase correction. Since the PA is operating close to or even beyond the compression point, the efficiency can be very high. Again, the limitation is the lack of an efficient dynamic power supply circuit with wide bandwidth.

2.3.4 Power-Level Tracking

To implement EER, ET, or EF, an efficient dynamic power supply circuit with a bandwidth wider than the RF modulated signal bandwidth is needed. For wideband applications such as 802.11 and W-CDMA, there are no commercially available products that possess the required bandwidth. Power-level tracking (PT), or slow-envelope tracking PAs, as shown in Figure 2.5, do not track the actual envelope of the signal; instead, they change the supply current, voltage, or both, based on the average power level [4, 10]. The average power level in CDMA or W-CDMA applications varies significantly slower than the envelope; therefore, slow-switching, but power-efficient, power supply circuits can be used.

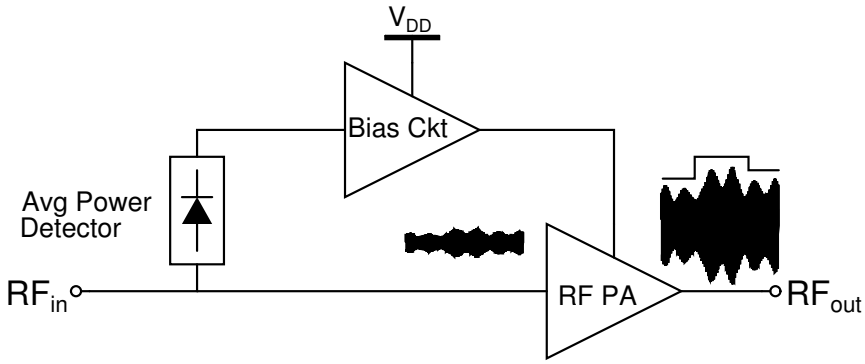


Figure 2.5 Block diagram of a power-level tracking PA.

A PT PA based on changing the supply current is demonstrated in [11]. PT PAs based on modulating the supply voltage are demonstrated in [5, 10]. Compared to the other dynamic biasing PAs previously mentioned, a PT PA is fairly easy to implement. The major disadvantage is the need for larger passive components because of the lower switching frequency. Since a PT PA only needs to track the average power levels, its implementation is very similar to power control circuits in GSM/GPRS power amplifiers. The work in [5, 10] used switching power converters to modulate the supply voltage efficiently, but switching power converters are usually not used in GSM/GPRS applications. GSM/GPRS power amplifiers can draw current as high as 2 A from the battery at peak power level; an inductor that can handle such current is usually large in size. A common method is to use a linear regulator between the PA and the battery. A highly saturated power amplifier can be modeled as a resistor, R, to the power supply. The current drawn from the battery can be written as

$$I_{bias} = \frac{V_{DD,PA}}{R}, \tag{2.12}$$

where $V_{DD,PA}$ is the supply voltage of the PA. The power consumed by the dynamic supply PA can be written as

$$P_{DC} = V_{BAT} I_{bias} = V_{BAT} \frac{V_{DD,PA}}{R}. \tag{2.13}$$

As $V_{DD,PA}$ is lowered by the linear regulator, overall power consumption is reduced. The power saved by a linear regulator is not as high as a switching power converter, but the cost of implementation is lower [10].

The concept of average efficiency shown in (1.3) makes the PT technique an attractive method to improve battery life for wireless applications with large PCR. For CDMA applications with 80 dB PCR, the PA is usually backed-off 20-30 dB from peak power. Using the PT technique with a switching regulator, the overall efficiency can be written as

$$\eta_{overall} = \eta_{SR} \frac{P_{out}}{V_{DD,PA} I_q}, \tag{2.14}$$

where η_{SR} is the efficiency of the switching regulator, Pout is the RF output power, $V_{DD,PA}$ is the regulated voltage supplied to the PA, and I_q is the quiescent current of the PA. If the regulated PA supply voltage is 20% of the battery voltage and the switching regulator efficiency is 80%, the overall efficiency can be increased by a factor of four. Since the efficiency at higher probable power levels is increased significantly, the average efficiency and battery life are increased. However, such improvement in battery life is paid at a price. First, PT PAs require the use of linear PAs. Since the efficiency of a switching regulator is never 100%, the peak efficiency of a PT PA is always lower than

the original linear PA. The reduction of peak efficiency may increase thermal stress on the power devices and require the utilization of heat sinks. Second, the switching regulator used in a PT PA as in [5] causes in-band interference. The switching frequency is usually chosen to be less than 1 MHz. For wideband applications such as CDMA and W-CDMA, the ripple voltage can be up-converted and interfere with the RF modulated signal. To limit such interference, the switching regulator must be carefully designed to have sufficient suppression of the ripple voltage.

2.3.5 Polar Modulation

The basic advantage of Kahn's EER technique is to use nonlinear, but efficient, amplifiers to amplify the envelope information and phase information separately. In Figure 2.3, an envelope detector and a limiter are used to extract the amplitude and phase data. To reduce circuit complexity, a DSP-based open-loop polar modulator was proposed in [51]. Since the baseband data are stored in the form of $I+Qi$, the envelope information can be easily extracted by taking the absolute value of the baseband data, and the phase information can be computed using the CORDIC algorithm.

In an EER PA, the non-ideality in the process of combining the split phase and envelope information decreases the overall linearity. Envelope feedback used in [17–19] reduces the delay and amplitude distortion, but it does not correct any phase distortion. By adding a phase feedback loop, the phase distortion can be corrected. A possible way to implement a polar-modulated PA is shown in Figure 2.6. The error between the input and output envelope signals controls the dynamic biasing circuit. The phases of the input and output signals are compared; with a VCO that provides the PA with constant-amplitude signal, a phase-locked loop is constructed.

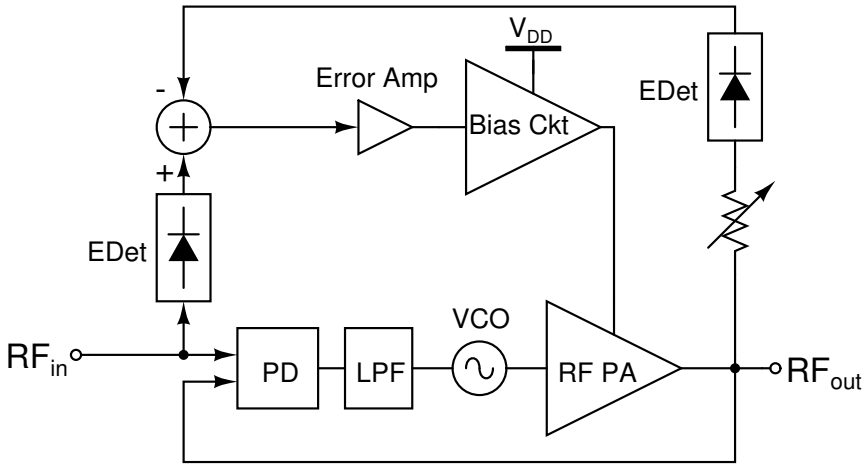


Figure 2.6 Block diagram of a polar modulated PA.

The modulation used in EDGE is 3π/8 shifted 8-PSK, which is not a constant envelope modulation scheme like GMSK used in GSM. To implement a linear PA for EDGE, the PA must be backed-off 6 dB from the compression point [25]. Either low efficiency must be tolerated or a separate PA is needed for GSM/EDGE dual-mode phones. By using polar modulation, overall linear amplification can be achieved with saturated GSM PAs at lower cost. Implementations of polar modulation have been shown in [7, 25–28] for GSM/EDGE applications. These implementations differ vastly in the way they combine the phase and envelope information. In [27], a high-speed linear regulator is used to modulate the drain of a saturated PA. In [25], the envelope and phase information are combined at the gate or base of the PA by varying the gate or base bias point. In [28], the envelope and phase information are combined at the PA input; the overall linear signal is created by varying the PA's driving signal. By using polar modulation, a single RF PA can be used in multiple wireless communication standards that use different modulation schemes. Besides cutting cost by reducing the number of PAs, the closed polar loop reduces the undesirable out-of-band emission so that

expensive off-chip surface acoustic wave (SAW) filters are no longer needed. A major challenge in designing a PA is to operate under voltage standing wave ratio (VSWR) variations. With polar modulation, the PA is able to maintain linearity under high VSWR without the use of an isolator [25]. Without the use of SAW filters and isolators, RF power loss can be reduced and the overall efficiency can be further increased.

2.3.6 Mode Switching

Mode switching PAs switch between different modes depending on the output power level. Dual bias mode PAs for CDMA applications are quite common for PAs currently on the market. For low output power levels, the bias current of the PA is reduced to conserve power [50]. A switched-gain PA is another kind of mode switching PA [29]. The switched-gain PA operates as a normal PA when the output power level is high. When the PA is backed-off from peak power, one stage is bypassed to reduce power consumption. Mode switching was also demonstrated in [30], where the output matching network is switched. The parallel amplification PA implemented in [31] switched between a high-power PA and a low-power PA that are in parallel.

Mode switching is the easiest way to enhance a PA's efficiency. Switching between different power levels can be easily implemented with a digital signal. Additional circuitry needed to implement mode switching can be integrated into the PA module. The main reason that mode switching is not preferred is the abrupt change. The basestation usually accomplishes phase estimation over several slots. The changes in the bias of a PA or even switching between two PAs can cause sudden change to the PA phase response. Any phase discontinuity can increase the possibility of losing the connection between the handset and the basestation [48].

2.4 Summary

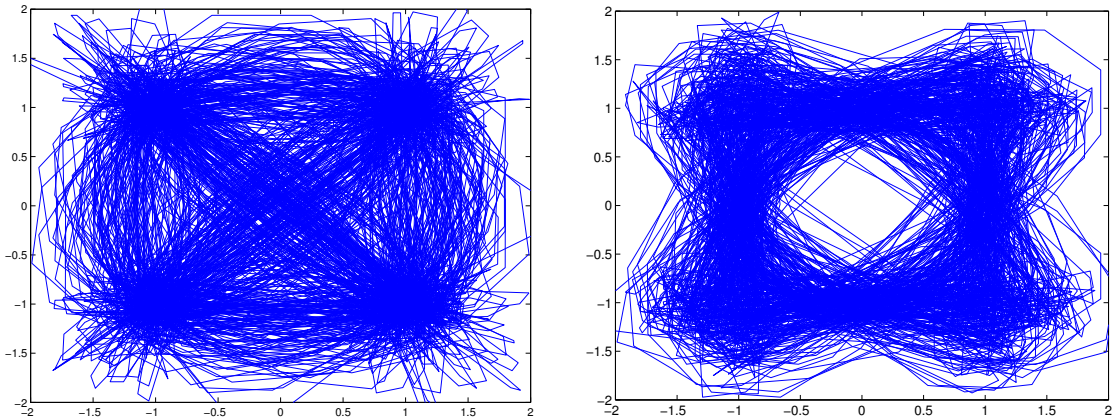
CMOS implementations of dynamic power supply IC for various dynamic power supply PAs have been shown in [19, 24, 32–34]. Wide bandwidth, high accuracy, high efficiency, and low cost have not been achieved concurrently. To implement a dynamic-biased PA for today's wide bandwidth wireless applications, the dynamic power supply circuit has to achieve all of them at the same time. Continuous and monotonic changes to the signal are also highly desirable since any step-change or spike can cause the connection to drop. Among all dynamic power supply schemes, polar modulation has the most benefits, with narrow bandwidth being its major limitation. The PT PA provides a low-cost solution with minimum additional circuitry to a fixed-biased linear PA. The PT technique may be another attractive solution for wideband and wide power control range applications such as W-CDMA and WiMax.

CHAPTER 3

AN EER PA USING A DELTA-MODULATED SUPPLY CIRCUIT FOR CDMA APPLICATIONS

3.1 Introduction

IS-95 is a CDMA standard widely used in the North America. For the reverse-link, from handset PA to basestation, offset QPSK (OQPSK) is used. In OQPSK, I(t) and Q(t) are delayed by half the clock period so the phase change is limited to 90º. This is unlike conventional QPSK used in IS-95 CDMA forward-link, which has a maximum phase change of 180º. By doing this, the envelope of an OQPSK signal never goes to zero and makes the design of PAs easier due to the reduced dynamic range requirements. The constellations of QPSK and OQPSK are compared in Figure 3.1. It was shown in [20], modulation standards without zero-crossing points, such as OQPSK, are more suitable for EER.



(a) Forward link (QPSK) (b) Reverse link (OQPSK)

Figure 3.1 IS-95 CDMA constellation.

In this work, an EER PA for cellular band IS-95 CDMA applications was implemented using a CMOS dynamic power supply IC with a 3 MHz bandwidth [35]. The design and implementation of the EER PA are discussed below, focusing mainly on the dynamic power supply IC, which is currently the major implementation barrier for an EER PAs. Measurement results using IS-95 CDMA signals are also shown in this chapter.

3.2 Supply Circuit Design and Implementation

The dynamic power supply IC consists of an lead-lag filter for compensation, a clocked comparator for quantization, output buffer to drive the load, and on-chip resistive feedback to define the gain. An off-chip low-pass LC filter was used to filter the unwanted aliasing component after sampling. Since the sampling frequency is very high, small off-chip component values could be used (L = 1 μH and C = 3 nF). The block diagram of the dynamic power supply circuit is shown in Figure 3.2. The dynamic power supply IC was implemented using a 0.5μm 2P3M CMOS process, and fabricated by AMI through MOSIS. The partial die photo and chip layout are shown in Figure 3.3 and Figure 3.4, respectively.

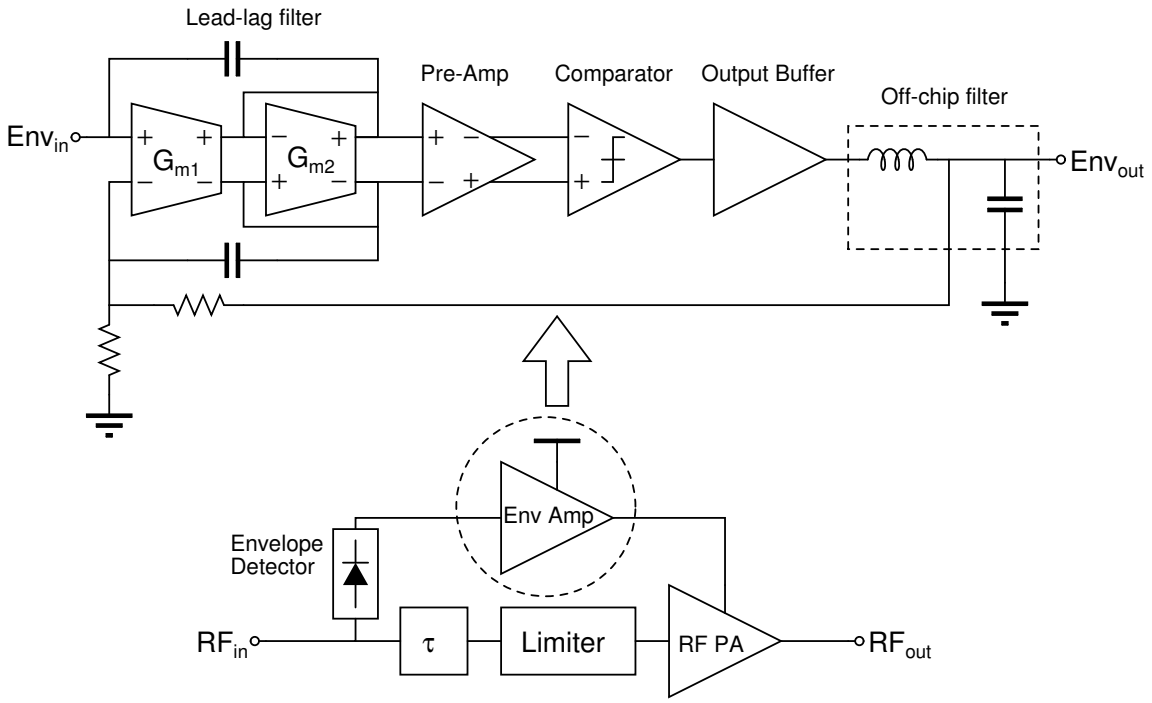


Figure 3.2 Block diagram of the dynamic supply circuit.

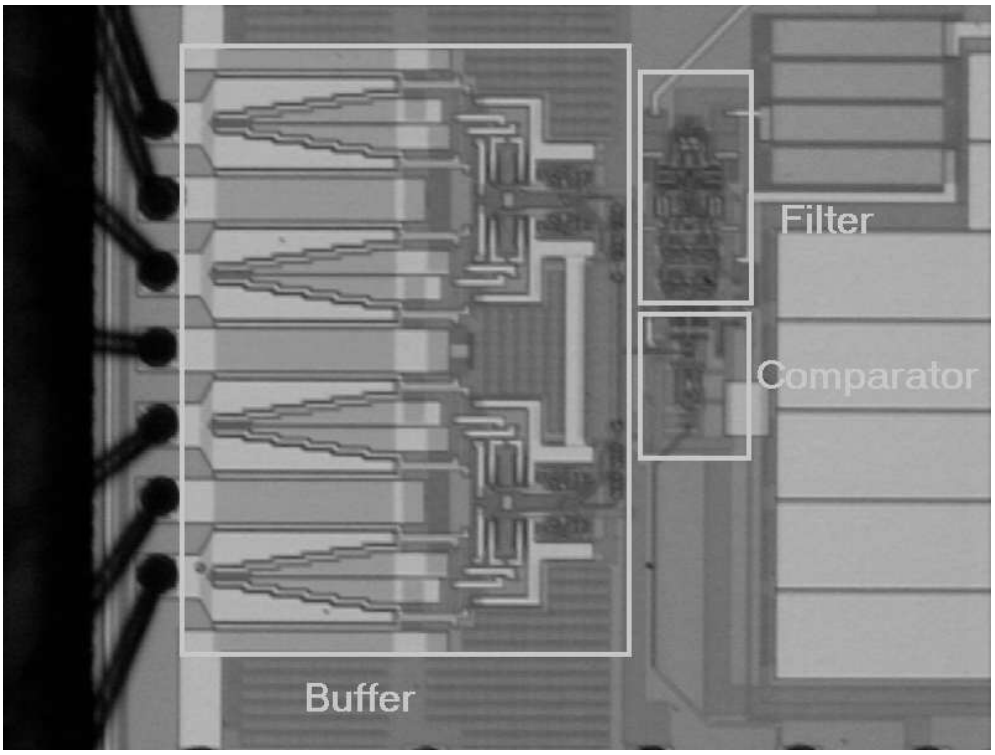


Figure 3.3 Layout of delta-modulated supply circuit.

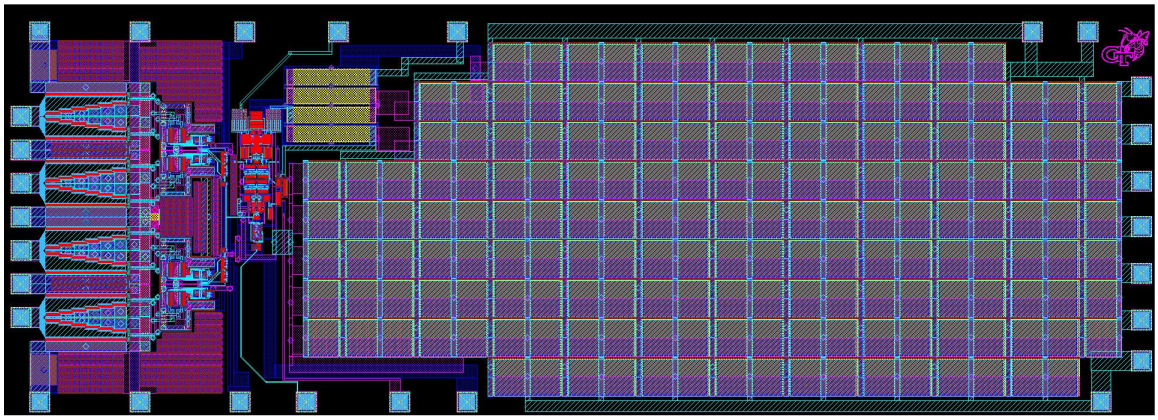
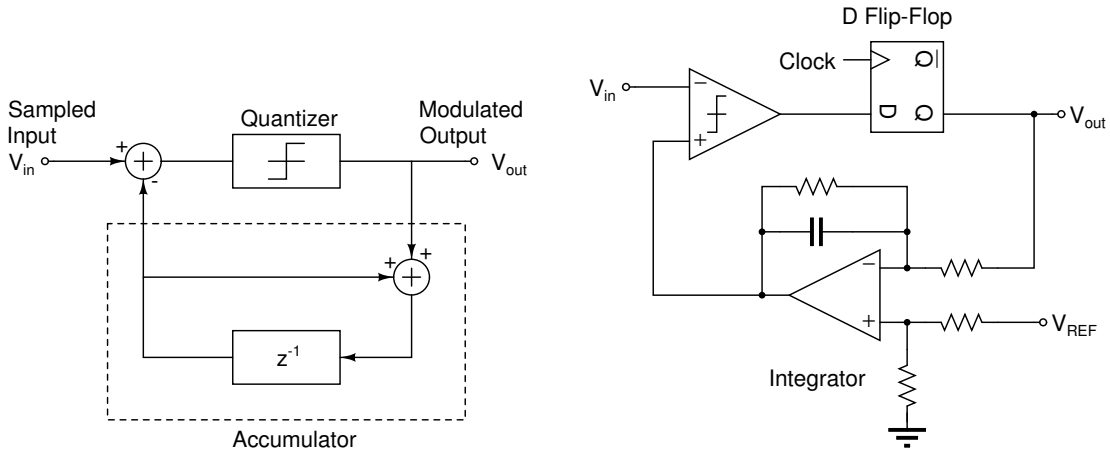


Figure 3.4 Partial die photo of delta-modulated supply circuit.

3.2.1 Delta Modulation

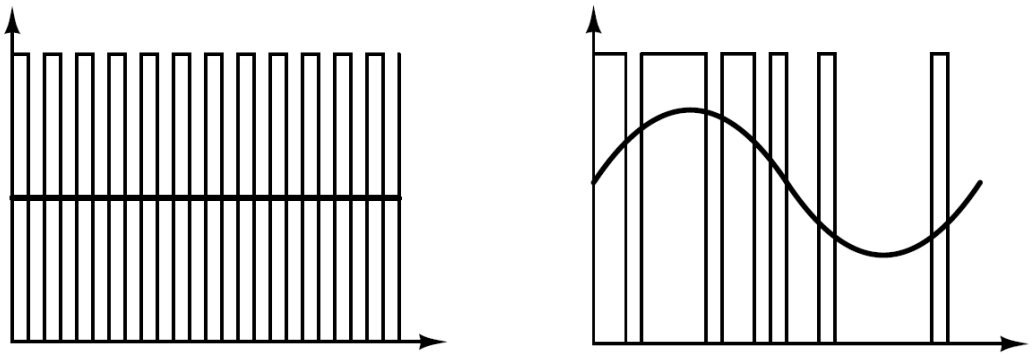
Delta modulation has been a widely used modulation technique for speech applications because of its simplicity and synchronous behavior. Instead of transmitting the complete amplitude information as in pulse-code modulation, only the difference is coded [36]. With a sufficient over-sampling ratio, delta modulation can achieve similar performance as pulse code modulation, with a much lower cost to implement. The basic block diagram of a delta modulator is shown in Figure 3.5.



(a) Block diagram (b) Circuit implementation

Figure 3.5 Basic block diagram and circuit implementation of a delta modulator.

Pulse-width modulation (PWM) has been the most widely used modulation technique for switching power supply circuits. In this work, delta modulation is chosen as in [19] for its simplicity. Unlike PWM, delta modulation codes the difference between the current output signal and input signal rather than the actual amplitude. For a delta modulator, the output can only change at the clock edges, but this does not necessarily mean it will change at all clock edges. Therefore, increasing the sampling frequency does not increase the switching loss significantly as in PWM. The worst case for a delta modulator is when the input is in the middle of the two output voltage levels. If the output voltage level is V_{DD} and 0, an input of around $V_{DD}/2$ will cause the output to change state at each clock edge leading to the highest switching loss possible. Delta modulation for the worst case and a typical sine wave is shown in Figure 3.6.

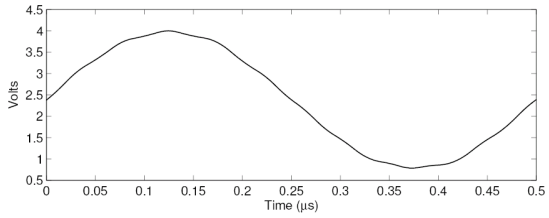


(a) Worst case (b) Typical

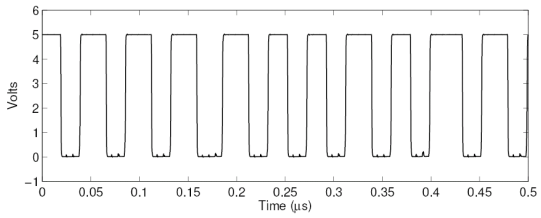
Figure 3.6 Comparison of delta modulation bitstream.

The simulation result of the implemented dynamic power supply circuit with a 250 mA current source load and 150 MHz sampling frequency is shown in Figure 3.7. The filtered output signal shown in Figure 3.6(a) is a 2 MHz, 3 V_{p-p} sinusoidal wave. The simulated efficiency for the sinusoidal wave was 80% and 56% for the worst case, as in Figure 3.6(a). It is apparent that for a typical signal, the amplifier is switching far less

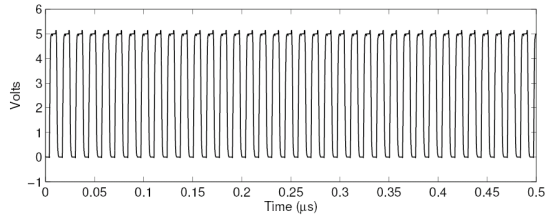
than in the worst case and the switching loss is less. The spectrum of the simulated 2 MHz, 3 V_{p-p} sinusoidal wave is shown in Figure 3.7(d). The noise resulting from quantization is 48 dB lower than the sinusoidal signal.



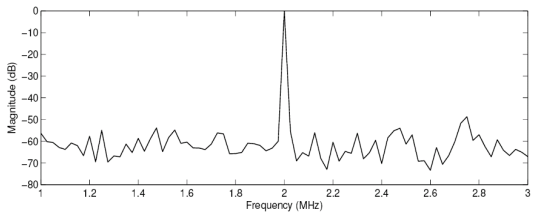
(a) Output 3 V_{p-p} sinusoidal wave



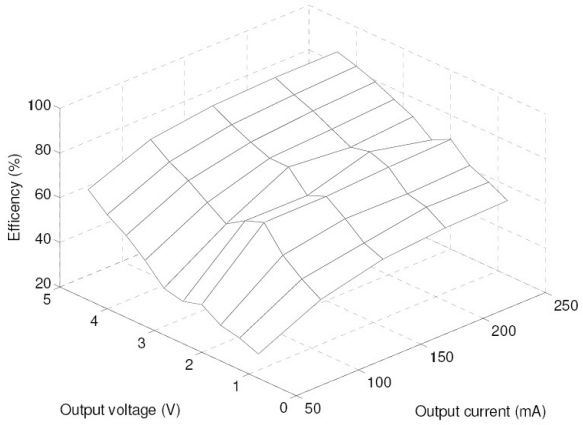
(b) Comparator output



(c) Worst-case comparator output



(d) Output spectrum



(e) Efficiency for various DC output

Figure 3.7 Simulation results of delta-modulated dynamic supply circuit.

3.2.2 Integrated Output Switches and Driver

The output buffer circuit, composed of the output switches and driving circuit, is used to create a replica of the comparator output to supply power to the RF PA. A fully integrated buffer circuit was used in this work. The major benefit of using a fully

integrated buffer is the reduction of package parasitics. If off-chip switches are used, on-resistance and static power loss can be reduced; however, additional bondwire inductance, lead inductance, and trace inductance between the off-chip switches and the driver will exist. Parasitic capacitances from the package and interconnections will also be introduced between the driver and the switches. The high-frequency square wave used to drive the switches will be distorted by the inherent low-pass behavior of the additional parasitics. The distorted driving signal will result in longer transition time and greater power loss. In addition, the increased transition time will create large propagation delay in the feedback loop and create stability problems. A non-overlapping driving signal is usually used for the output switches in switching power supply circuits to prevent shoot-through current to exist. Such a precaution is to protect the output switches from burning and consuming power. As the switching frequency increases, the power loss resulting from shoot-through current becomes significant in the driver composed of cascaded inverters, especially the last few stages where the transistor sizes are close to the output switches. By using a tree-like buffer structure as in Figure 3.8 and a slightly more complicated logic control circuit, a non-overlapping driving signal can be generated in the last few stages of the output buffer circuit. Such a buffer structure possesses higher efficiency when switching at a higher rate.

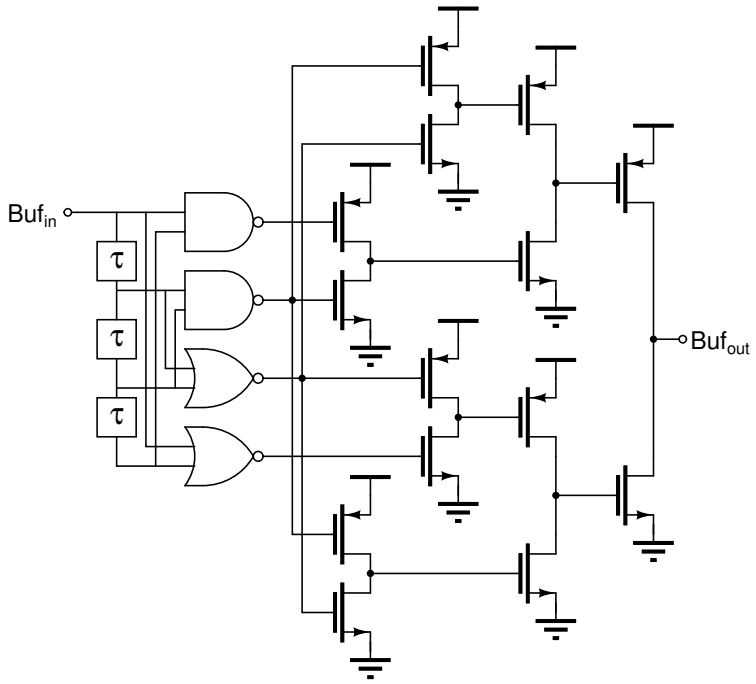


Figure 3.8 Tree-like buffer structure for reduced power loss.

3.2.3 Comparator

The digital buffer circuit is driven by a clocked comparator. Since the comparator can only change state at the clock edges, the comparator can be simply implemented by a preamplifier and a D-type flip-flop. The synchronous comparator uses a structure similar to the dual-edge triggered D-type flip-flop shown in [37]. Using a dual-edge triggered D-type flip-flop, each half-circuit only needs to operate at 75 MHz. The schematic is shown in Figure 3.9.

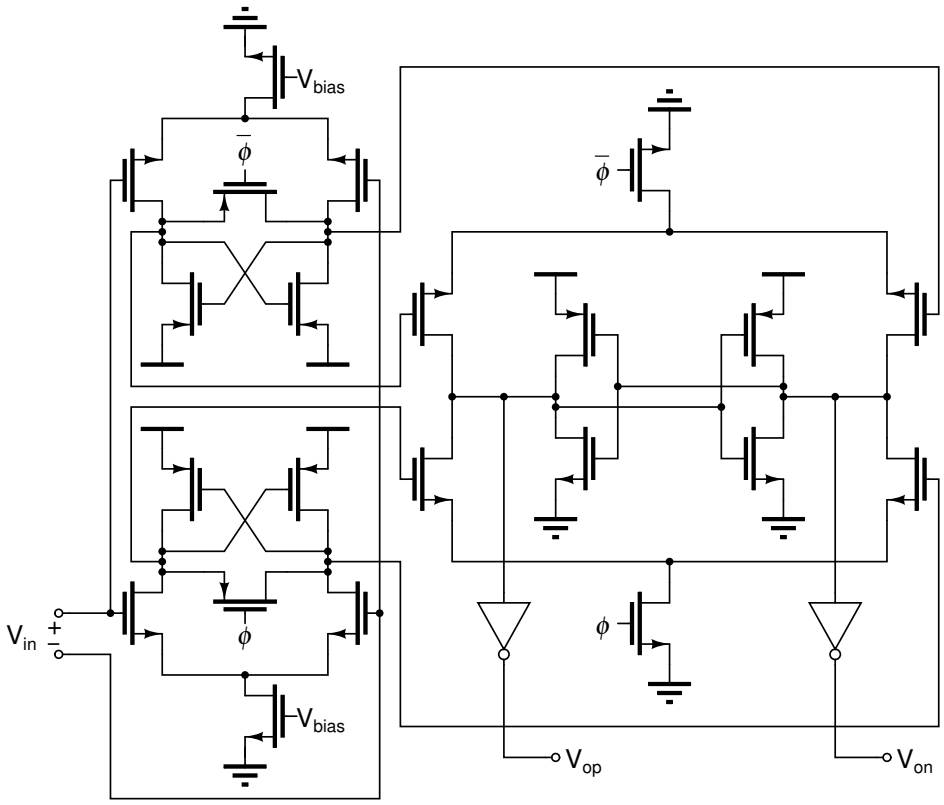


Figure 3.9 Synchronous comparator with low delay.

The main source of power consumption in this stage is the static current consumed in the preamplifier. The comparator only needs to drive a very small capacitive load, the input of the buffer circuit, so a small transistor size can be used and power consumption is low even with high clock frequency.

3.2.4 Delay Compensation and Feedback Stability

The modulated signal at the input of the EER PA is split into two different paths. After being processed separately in the two paths, the signals are combined at the RF PA. If the signals in the two paths are not synchronized, out-of-band emission will be generated and adjacent channel power ratio (ACPR) is degraded [21]. The amplitude or envelope path usually has more delay than the phase path. To synchronize the two paths,

either delay has to be deliberately added to the phase path or delay has to be reduced in the amplitude path. The major source of delay in the envelope path comes from the low-pass filter at the output of the digital buffer that is used to filter the unwanted aliasing components resulting from sampling. The power amplifier load is modeled as a current source in parallel with a resistor, R_{ds}, as shown in Figure 2.2. The frequency response of the output filter can be written as

$$A_{low-pass}(\omega) = \frac{R_{ds}}{R_{ds} + j\omega L - \omega^2 R_{ds} LC}, \tag{3.1}$$

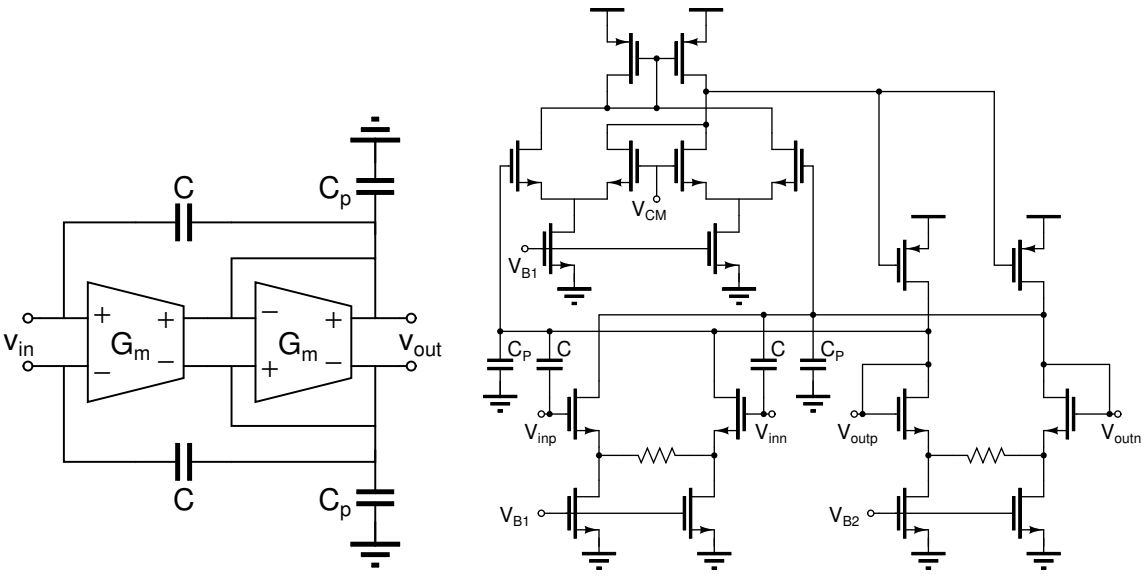
and the delay can be written as

$$\tau(\omega) = -\frac{d\phi}{d\omega} = \frac{R_{ds} L(1+\omega^2 LC)}{R_{ds}{}^2(1-\omega^2 LC) + \omega^2 L^2}. \tag{3.2}$$

Since R_{ds} varies for different biasing conditions, the delay caused by the filter is frequency dependent and load dependent such that the delay can not be compensated by a simple transmission line delay in the phase path. An alternative is to reduce the delay by using feedback so the overall delay of the filter can be reduced by the loop gain [19]. The main problem in the implementation of feedback is the existence of two conjugate poles generated by the LC low-pass filter. To ensure stable feedback, either the bandwidth has to be sacrificed by adding a low-frequency pole or a LHP zero has to be added to the feedback loop to reduce the overall phase shift. To achieve wide bandwidth, the latter was chosen. A lead-lag G_m–C filter shown in Figure 3.10 was used to generate a low frequency LHP zero to compensate for the phase shift caused by the output filter. The filter has a transfer function of

$$A_{lead-lag}(\omega) = \frac{2G_{m1} + j\omega C_f}{2G_{m2} + j\omega(C_f + C_p)}. \tag{3.3}$$

The zero location, $2G_{m1}C_f$, is chosen close to the frequency of the two conjugate poles, and the pole location , $2G_{m2}(C_f+C_p)$, is chosen to be several times greater than the zero so the phase shift at the frequency of interest is negligible. The capacitor C_f was implemented with an on-chip poly-poly capacitor. Parasitic poly-substrate capacitance, C_p, decreases the pole frequency, $2G_{m2}(C_f+C_p)$, and causes undesirable phase delay. The ratio between G_{m2} and G_{m1} has to be chosen large enough to reduce such effect. Because G_{m2} is greater the G_{m1}, the gain of the lead-lag filter is less than one. A voltage amplifier is added at the output of the lead-lag filter to compensate for the gain loss. The bandwidth of the voltage amplifier has to be high enough so its phase shift at the zero location of the lead-lag filter is negligible.



(a) Block diagram (b) Transistor implementation

Figure 3.10 Implementation of lead-lag filter for phase compensation.

3.3 Measurement Setup

A Sirenza SHF-0289 1 W GaAs/AlGaAs HFET is used as the RF power amplifier of the EER PA. The reverse-link IS-95 CDMA signal is generated using an Agilent 4432B vector signal generator. Since the signal generator is output power is not sufficient to drive the RF PA deep into saturation, a Sirenza SHF-0189 0.5 W HFET is used as a pre-amplifier. A Mini-circuit power splitter is used to split the input signal into an envelope path and a phase path. The envelope signal is detected using an envelope detector with schematic shown in Figure 3.11. The envelope detector is a high-speed diode detector circuit with a third-order Bessel filter to filter out the high frequency unwanted components. The phase shift caused by the envelope detector's filter can be compensated by a transmission line delay inserted in the RF path. A balanced detector was used to reduce reverse IMD that would be injected at the PA input. An RF attenuator is inserted in front of the envelope detector to tune the gain of the envelope signal. A photograph of the measurement setup is shown in Figure 3.12.

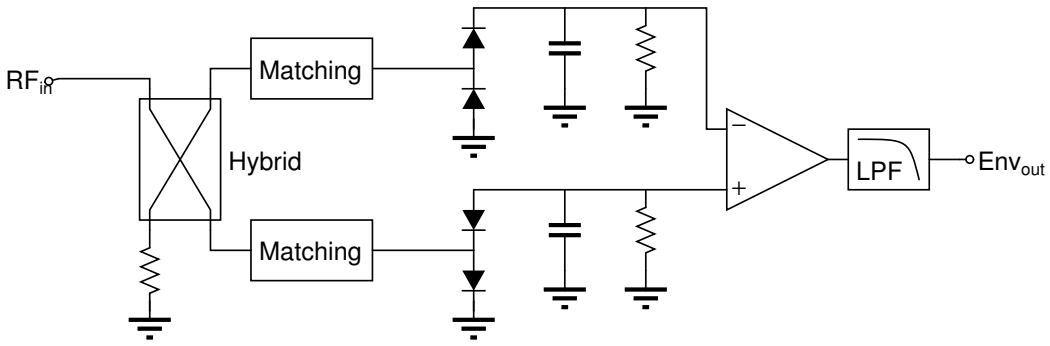


Figure 3.11 Circuit implementation of the envelope detector.

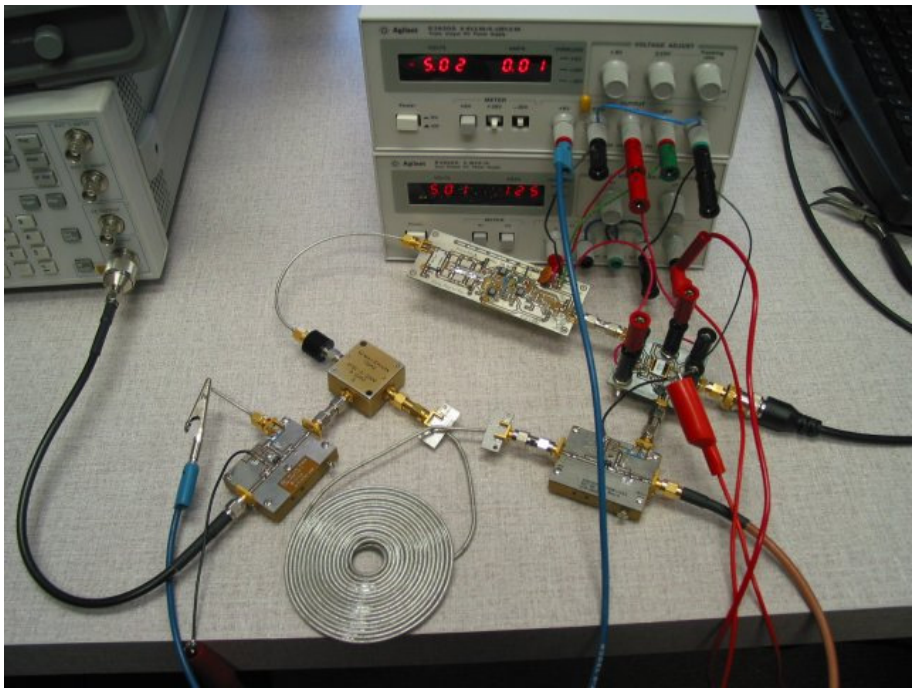


Figure 3.12 Measurement setup for CDMA EER PA.

3.4 Measurement Results

3.4.1 Dynamic Power Supply Circuit

The dynamic power supply chip operates at a clock frequency of 150 MHz and achieved a bandwidth of about 3 MHz. With a 5 V supply voltage, the chip was capable of supplying 0.5 V to 4.5 V to the load with efficiency up to 80% at peak output current. The output spectrum of a 2 MHz, 3 V_{p-p} sinusoidal signal is shown in Figure 3.13. The performance of the dynamic power supply circuit is summarized in Table 3.1.

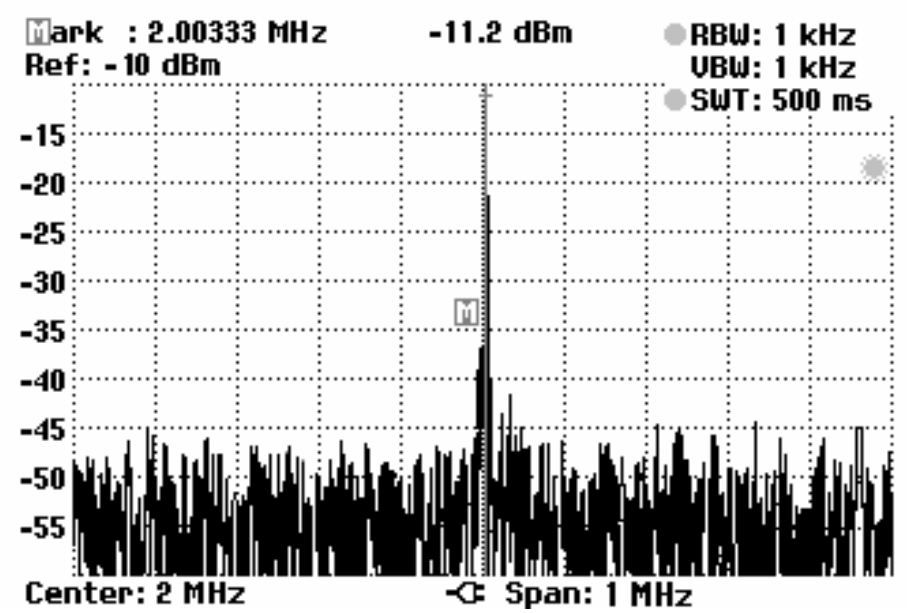


Figure 3.13 Measured spectrum of dynamic supply circuit with an 18 Ω load.

Table 3.1 Performance summary of delta-modulated supply circuit

Supply Voltage	5 V
Output Voltage Range	0.5 V ~ 4.5 V
Maximum Output Current	250 mA
Clock Frequency	150 MHz
Bandwidth	3 MHz
Peak Efficiency	80% (@Pout=25dBm)
Static Power Consumption	60 mW
Gain	4 V/V

3.4.2 Envelope Elimination and Restoration Power Amplifier

The power amplifier (Sirenza SHF-0289) used in this EER PA implementation was designed to work at a supply voltage of up to 7 V. Because of the limited output

voltage of the dynamic power supply circuit, the power output capability is slightly reduced. A limiting amplifier, as shown in Figure 2.3 is usually used to create a constant envelope driving signal for the PA to reduce AM-PM distortion [19]. In this implementation, such distortion was not severe so a limiting amplifier is not used and the RF PA is operated in the deep saturation region. Instead of linearity, quantization noise and switching noise are the major limitations of ACPR performance. The envelope detector is a diode detector with a third-order linear phase filter. A transmission line delay was used to compensate the constant delay in the envelope detector. Measurements using IS-95 reverse-link signal have been performed. The performance of the EER PA system has been measured and compared with a fixed biasing PA having a constant drain voltage of 4.5 V. An efficiency comparison of the PAs is shown in Figure 3.14. Compared to the fixed biasing PA, the EER PA shows higher efficiency over the entire range of output power level. Using the EER technique, an efficiency improvement of up to 17 % can be achieved. For lower input power, the dynamic power supply circuit supplies a constant 0.5 V to the drain of the RF PA. With a constant 0.5 V supply, the PA operates in the linear region and the PA is actually no longer an EER PA.

For fixed biasing PAs, the efficiency decreases dramatically when the output power is backed-off from P_{1dB}. For EER PAs, the main efficiency limitation is the modulator that drives the output buffer, which consumes static power. When the RF output power is low, the static power consumed by the dynamic power supply circuit becomes comparable to the RF output power and leads to lower overall efficiency. For this implementation, the modulator consumed 60 mW static power and the output buffer

circuit and the RF PA consumed a total of 45 mW when the dynamic power supply circuit supplies constant 0.5 V.

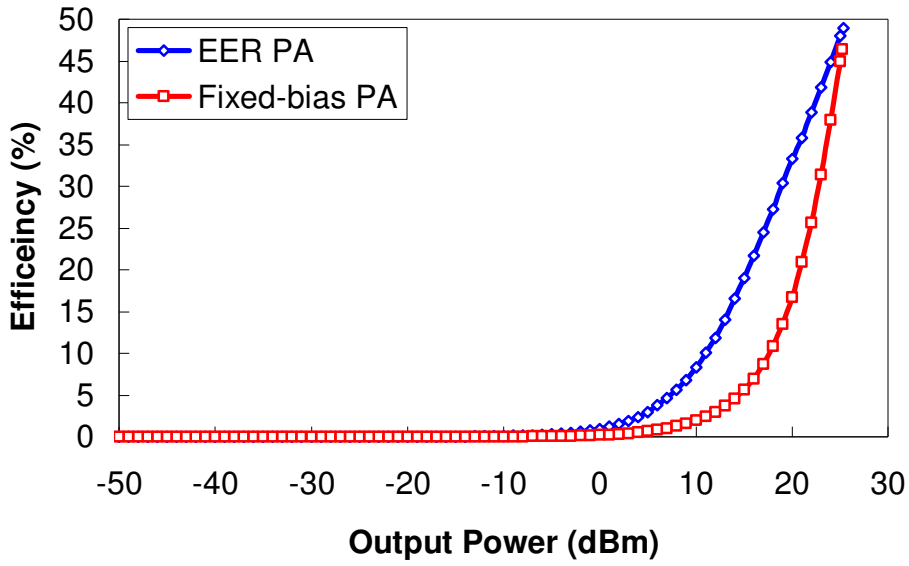


Figure 3.14 Efficiency comparison of EER PA and fixed biasing PA.

The IS-95 CDMA standard requires the handset power amplifier to change output power in 1 dB steps every 1.25 ms. The power amplifier of a CDMA handset can have a dynamic range up to 80 dB. In real operation, the PA output power has a distribution function shown in Figure 1.2. To assess the performance of the EER PA in this work, the average efficiency of the EER PA and fixed biasing PA can be calculated using the probability distribution function shown in Figure 1.2(b).

The power level of CDMA PAs are adjusted in 1 dB steps; therefore, (1.3) can be rewritten as

$$\overline{\eta}_d = \frac{\sum P_{out,W}(P_{out,dB})\,p(P_{out,dB})}{\sum P_{dc,W}(P_{out,dB})\,p(P_{out,dB})}, \tag{3.4}$$

where $P_{out,W}(P_{out,dB})p(P_{out,dB})$ is defined as the weighted output power for power level

$P_{out,dB}$ and $P_{dc,W}(P_{out,dB})p(P_{out,dB})$ is defined as the weighted DC power consumption for power level $P_{out,dB}$. To determine the average efficiency, the weighted output power and weighted DC power consumption is calculated and shown in Figure 3.15 and Figure 3.16 using the urban and suburban probability distribution function, respectively [3-5]. The results are shown and compared with other reported dynamic-biased PAs for CDMA applications in Table 3.2.

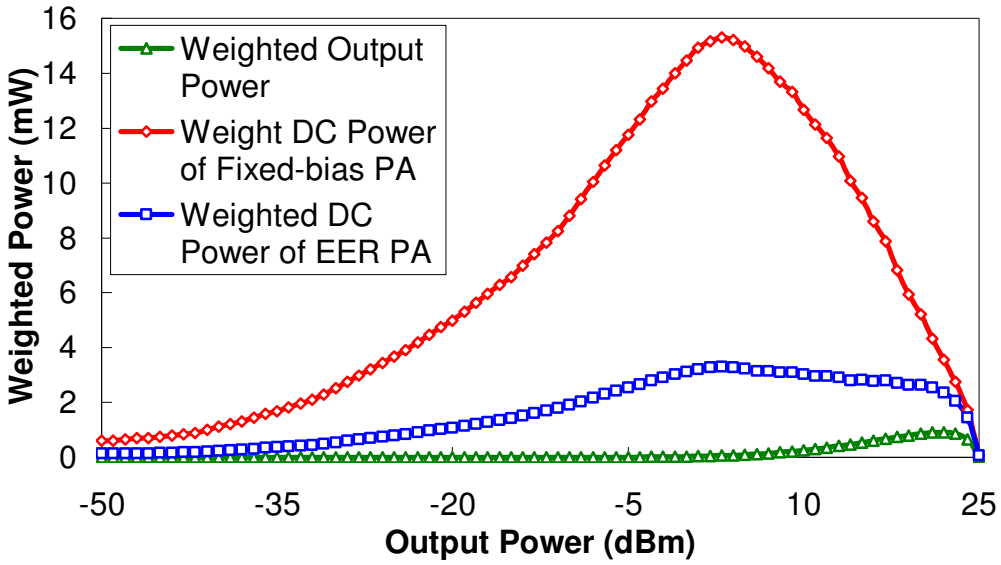


Figure 3.15 Comparison of weighted power using urban area probability distribution function.

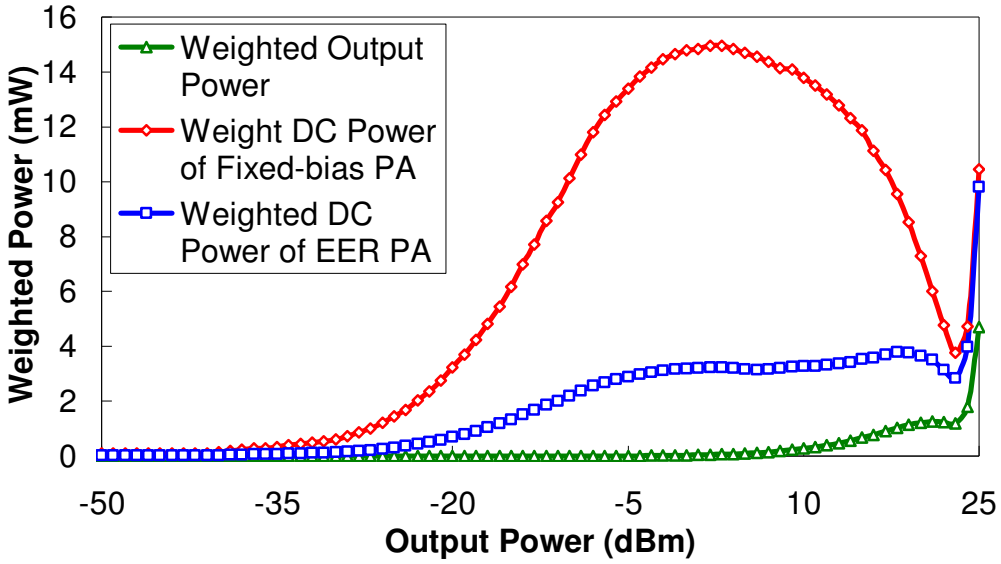


Figure 3.16 Comparison of weighted power using suburban area probability distribution function.

Table 3.2 Efficiency comparison of dynamic-biased PAs for CDMA applications

	Topology	Fixed-Biased PA Efficiency	Dynamic-Biased PA Efficiency
Staudinger [4]	PT	2.2 %	11.2 %
Hannington [22]	ET	3.89 %	6.38 %
Sahu [5]	PT	1.53 %	6.78 %
This work (urban)	EER	2.09 %	8.49 %
This work (suburban)	EER	3.76 %	13.73 %

The overall gain of the EER PA is mainly determined by the envelope path. The Sirenza RF PA used in this implementation had around 20 dB of linear gain. For this implementation of the EER PA, the gain is around 12 dB. The gain measurement results are shown in Figure 3.17. At low output power level, the PA no longer operates as an EER PA and the gain begins to decrease as the HFET enters the ohmic region. The

lowered gain resulting from the changing PA drain voltage has also been discussed in [22] and [5]. The ACPR performance of the EER PA and the fixed biasing PA has been measured over a range of output power levels. The measurement result is shown in Figure 3.18. As expected, the ACPR of the fixed biasing PA improved when the PA is backed-off from the P_{1dB} point, whereas the ACPR of the EER PA stays relatively constant. For high output power, the EER PA shows considerably better ACPR performance than the fixed biasing PA that operates close to the P_{1dB} point.

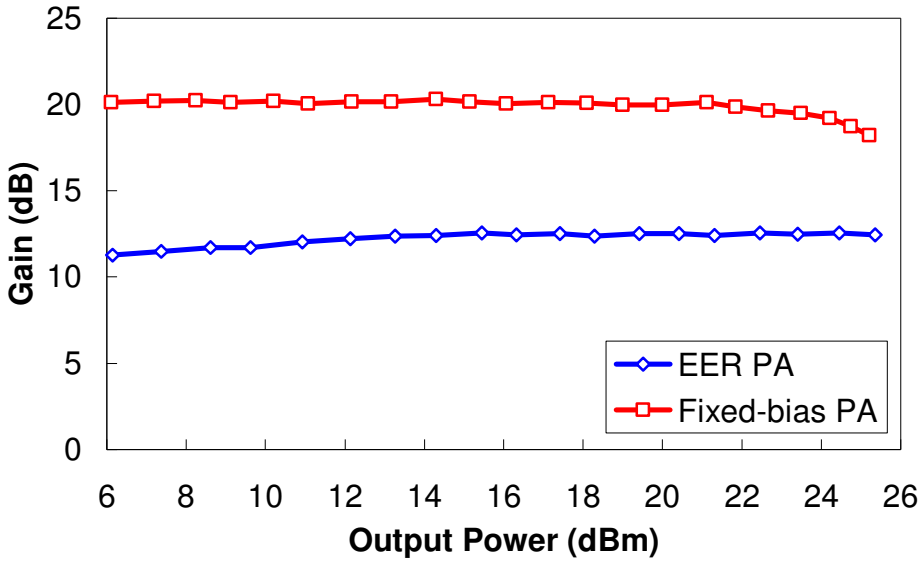


Figure 3.17 Gain measurement of EER PA and fixed biasing PA.

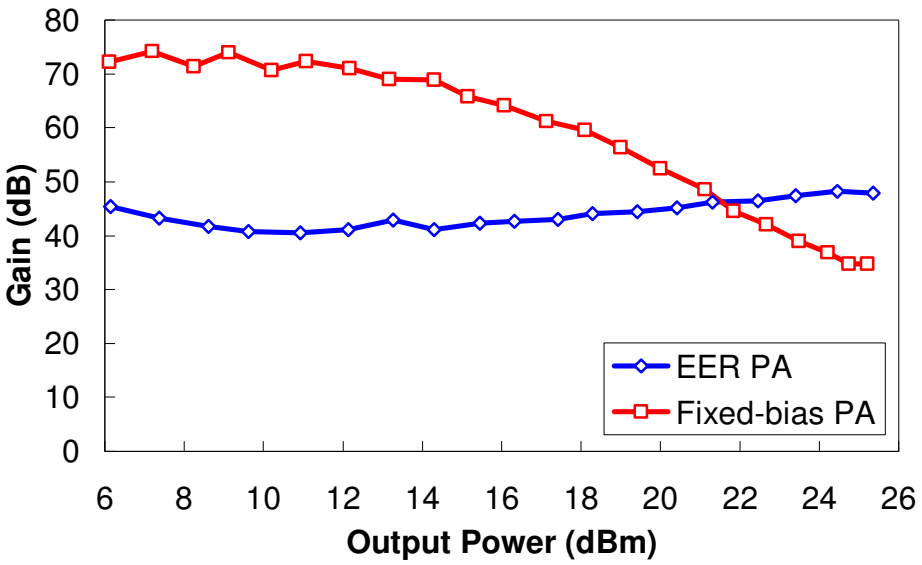


Figure 3.18 ACPR measurement results of EER PA and fixed biasing PA.

The output spectrum of the fixed biasing PA and the EER PA with and without delay synchronization at 25 dBm output power using IS-95 signal are compared in Figure 3.19. Measurements of the performance are summarized in Table 3.3. At 25 dBm output power, the fixed biasing PA is operating beyond P_{1dB} so increased power can be seen in the adjacent channels. By applying the EER technique, linearity can be dramatically improved even without delay synchronization using a transmission line. However, without delay synchronization, the output spectrum is highly asymmetric. With delay synchronization, the efficiency of the EER PA is slightly reduced because the transmission line delay has attenuation and decreases the power magnitude at the RF PA input, but the output spectrum is close to being symmetric and passes the ACPR requirement for IS-95.

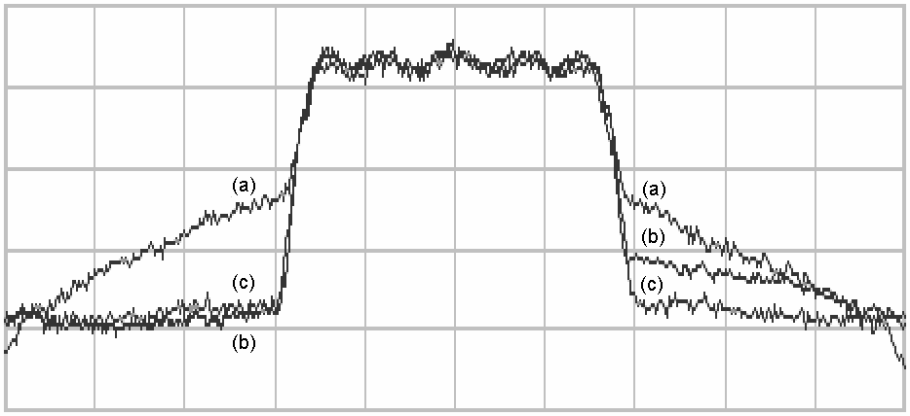


Figure 3.19 Comparison of measured output spectrum of (a) Fixed biasing PA, (b) EER PA without synchronization, and (c) EER PA with synchronization.

Table 3.3 Summary of EER PA performance at 25 dBm output power

	Lower ACPR	Upper ACPR	Efficiency
Fixed biasing PA	34.7 dBc	35.1 dBc	46 %
EER PA (with synchronization)	48.3 dBc	47.9 dBc	48 %
EER PA (without synchronization)	48.9 dBc	42.5 dBc	51 %

Delta modulation uses a single-bit quantizer to quantize the analog signal. Quantization noise is generated after quantization. The high-frequency component of the quantization noise is filtered out by the off-chip L-C filter. The in-band quantization noise will create a noise floor-like spectrum, as shown in Figure 3.7(d) and Figure 3.13. After combining the phase and amplitude signal, the noise is up-converted to the carrier frequency and sets a limitation to the ACPR. In Figure 3.19, the large slope in the adjacent channel was not significant when the EER technique with synchronization is applied. Instead, the power in the adjacent channel is close to being flat. From simulation results, the power level of the quantization noise remains approximately the same with

changing output signals. Theoretically, if the noise is up-converted to the carrier frequency, the ACPR will degrade 1 dBc when the output signal is lowered by 1 dB. However, in the measurement result shown in Figure 3.18, the ACPR decreases more slowly than the output signal power. The main reason for this is the substrate coupling of noise. To reduce parasitics that limit the operation frequency of the dynamic power supply circuit, the analog portion of the chip is in close proximity to the output buffer circuit. Because the output buffer circuit is sinking and sourcing a large amount of current and alternating at fairly high frequency, the substrate becomes very noisy. By comparing Figure 3.7(d) and Figure 3.13, it is obvious that the noise level increased by more than 10 dB. The noisy substrate may disturb the analog portion of the chip and lead to incorrect bits at the comparator output. The single-well process used in implementing the dynamic power supply circuit does not provide very good isolation between the analog and digital portions of the chip. Changing to a more advanced isolated p-well process may solve this problem and further improve the ACPR. The worst-case ACPR occurs at around 10 to 12 dBm output power and it is caused by the limited dynamic range of the envelope detector used. The envelope detector has a dynamic range of 20 dB, and the signal is undetectable for lower power level and causes the dynamic power supply circuit to supply a constant 0.5 V to the PA. The output power of 10 to 12 dBm is right at the transition and has the worst linearity.

3.5 Summary

A CMOS dynamic power supply IC with 3 MHz bandwidth and an efficiency of up to 80% has been designed and implemented. Low power consumption and wide bandwidth have been achieved at the same time by using delta modulation and low-

power G_m-C filters. The mixed signal IC proposed has high bandwidth, high accuracy, high power output, and high efficiency, and is compatible for use in an EER architecture. Using the dynamic power supply IC, a cellular band CDMA EER PA was designed, fabricated, and tested. The EER PA achieved 48% efficiency with 25 dBm output power while achieving an ACPR of 47.9 dBc. Compared to a fixed biasing PA, the PA's overall efficiency can be increased by up to 17% over a wide range of output power.

Using the output power probability distribution function of IS-95 CDMA to calculate the average efficiency, it was shown that the EER technique can increase the average efficiency by approximately four times. By using the EER technique, both the peak efficiency and average efficiency can be significantly improved. High peak efficiency reduces the thermal stress on the power transistors and obviates the need for a heat sink, whereas the high average efficiency leads to longer battery life. The increased output power leads to a smaller power transistor size and can reduce the cost of a PA.

CHAPTER 4

AN EER PA USING A DUAL-PHASE PWM SUPPLY CIRCUIT FOR W-CDMA APPLICATIONS

4.1 Introduction

The EER technique is a viable solution of achieving both high peak efficiency and high average efficiency. With the worldwide cellular phone service evolving toward 3G, wider bandwidth is also desirable. To improve the noise performance of an EER PA, a dual-phase PWM supply circuit is proposed. Using a multi-phase PWM supply circuit, greater bandwidth can be achieved with multiple slow, but efficient PWM supply circuits. Since each phase only needs to supply part of the output current, inductors with lower current rating can be used. Inductors with lower current rating are usually smaller in size and lower in cost, which make them more suitable for use in a wireless handheld device. The high effective switching frequency also makes it possible to use small sized ceramic capacitors for filtering.

A dual-phase PWM supply circuit is designed and implemented using AMI 0.6μm 2P3M CMOS process and packaged in a Kyocera CLCC28 package. The dual-phase PWM supply circuit is characterized together with a Sirenza SHF-0289 GaAs/AlGaAs HFET power transistor to implement an EER PA. A gain compensation FIR filter is implemented digitally using the characterization data to correct for the frequency-dependant gain error of the dual-phase PWM supply circuit. A crest factor reduction technique is also used to reduce the peak envelope power and increase both the average

output power and efficiency. To cover the whole power control range required for W-CDMA, PT technique is used in conjunction with EER technique to increase the inherent low dynamic range of a conventional EER PA.

4.2 System Level Requirements of EER PA for W-CDMA

The implementation of EER PAs has been limited to NADC applications with 30 kHz channel bandwidth because of the lack of power-efficient wideband dynamic supply circuits. Linear regulators were used in [27] and [43] for the dynamic supply; however, efficiency increase is limited, as shown in (2.3). It is desirable to have a switching regulator with sufficiently high bandwidth to implement an EER PA for wideband applications such as W-CDMA. Besides bandwidth, the other major limitation of an EER PA is the delay mismatch between the envelope path and the phase path. This section discusses the limitations of EER PA and system level requirements to pass the W-CDMA specification.

4.2.1 W-CDMA Modulation and Power Amplifier Requirements

The W-CDMA standard is defined by the technical body called the 3rd-Generation Partnership Project (3GPP). It is a successor of the widely used GSM standard. The channel spacing is 5 MHz. Unlike IS-95 CDMA, W-CDMA uses orthogonal complex quadrature phase shift keying (OCQPSK), which is also know as hybrid phase shift keying (HPSK) for reduced PAR such that the amount of PA back-off can be reduced and hence increase PA efficiency [48]. Special orthogonal codes are used to reduce the possibility of zero-crossing in the constellation and thus reduce the PAR [38].

The radio transmission and reception requirements are defined in chapter 25.101 of the 3GPP technical specification. The operating frequency for each band and the

maximum subscriber equipment output power are summarized in Table 4.1. The power amplifier is required to pass the out-of-band emission and spurious emission specifications. For the out-of-band emission specification, the spectrum is required to pass the spectral mask shown in Figure 4.1 (assuming 30 kHz measurement BW) and the ACLR specification shown in Figure 4.2. For frequencies more than 12.5 MHz away from the carrier frequency, the spurious emission specification must be passed. In this work, the EER PA is designed for Band V (824 MHz – 849 MHz) and Band VI (830 MHz – 840 MHz) power class 4 (21 dBm). The spurious emission requirements are summarized in Table 4.2.

Table 4.1 W-CDMA operating frequency and maximum output power

Operating Band	**Uplink Frequency**	**Power Class 1**	**Power Class 2**	**Power Class 3**	**Power Class 4**
Band I	1920-1980 MHz	+33 dBm	+27 dBm	+24 dBm	+21 dBm
Band II	1850-1910 MHz	-	-	+24 dBm	+21 dBm
Band III	1710-1785 MHz	-	-	+24 dBm	+21 dBm
Band IV	1710-1755 MHz	-	-	+24 dBm	+21 dBm
Band V	824-849 MHz	-	-	+24 dBm	+21 dBm
Band VI	830-840 MHz	-	-	+24 dBm	+21 dBm
Band VII	2500-2570 MHz	-	-	+24 dBm	+21 dBm

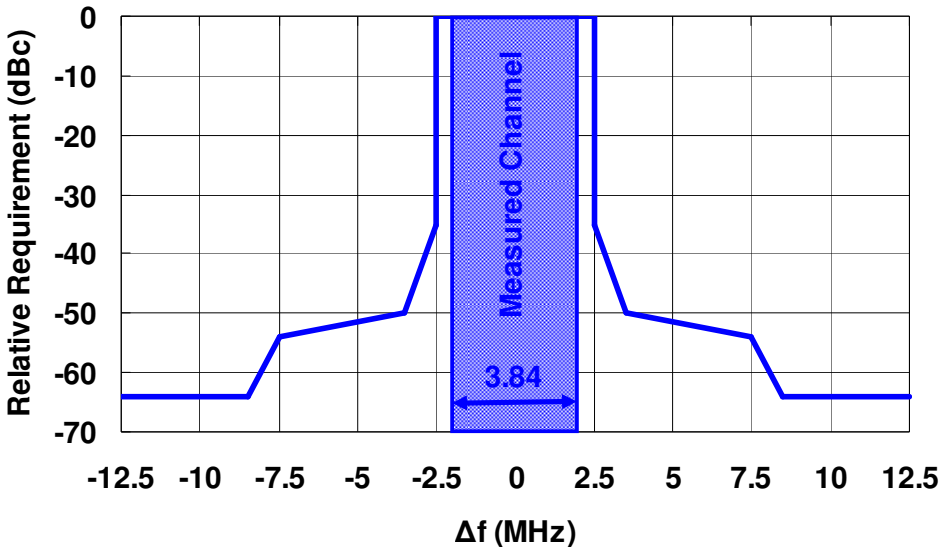


Figure 4.1 Spectral mask for W-CDMA.

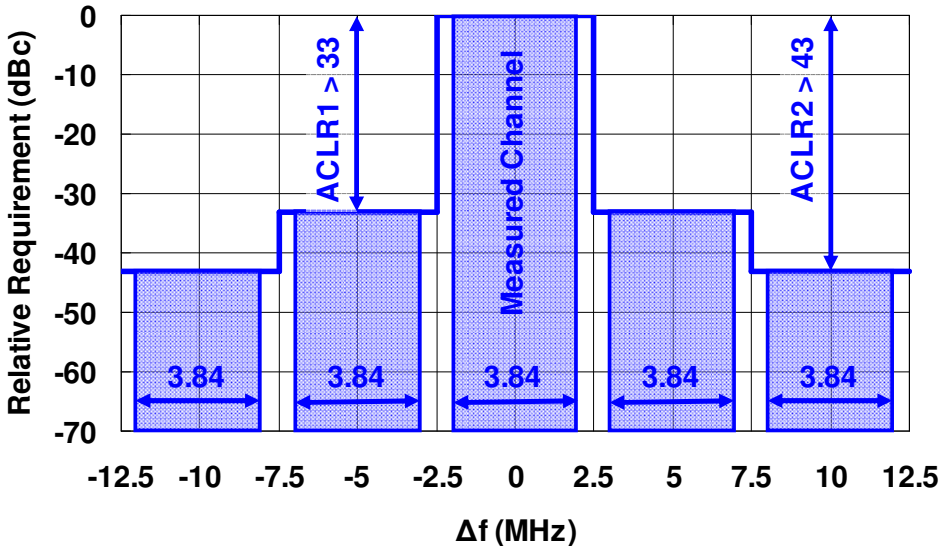


Figure 4.2 W-CDMA ACLR specifications.

Table 4.2 Spurious emission requirements for W-CDMA band V and VI

Frequency Bandwidth	Measurement BW	Requirement
9 kHz ≤ f < 150 kHz	1 kHz	-36 dBm
150 kHz ≤ f < 30 MHz	10 kHz	-36 dBm
30 MHz ≤ f < 1000 MHz	100 kHz	-36 dBm
1 GHz ≤ f < 12.75 GHz	1 MHz	-30 dBm
869 MHz ≤ f ≤ 894 MHz (V)	3.84 MHz	-60 dBm
1930 MHz ≤ f ≤ 1990 MHz (V)	3.84 MHz	-60 dBm
2110 MHz ≤ f ≤ 2155 MHz (V)	3.84 MHz	-60 dBm
875 MHz ≤ f ≤ 888 MHz (VI)	3.84 MHz	-60 dBm
1884.5 MHz ≤ f ≤ 1919.6 MHz (VI)	300 kHz	-41 dBm
2110 MHz ≤ f ≤ 2170 MHz (VI)	3.84 MHz	-60 dBm

For the implementation of an EER PA using switching regulators, the switching frequency should be carefully chosen. Unlike switching regulators in PT PAs that create in-band interference, the switching frequency of an EER PA is much higher to achieve the required bandwidth. Hence, spurious emission becomes a greater concern. For a conventional single-phase PWM switching regulator, the circuit is sampling at the switching frequency and aliasing will take place at integer multiples of the switching frequency. The aliasing components must be sufficiently suppressed by a filter such that the spurious emission specifications can be met.

In this work, a dual-phase PWM switching regulator is used for simplicity, while more phases can be used with the trade-off of added circuit complexity. If the switching

frequency for each phase is f_s, the switching regulator has an effective switching frequency of 2 f_s. The aliasing components at odd multiples of f_s are cancelled if the two phases are exactly matched. However, in realistic implementations, it is never possible to have the two phases exactly matched. Therefore, in addition to careful matching, sufficient attenuation needs to be provided by the filter.

4.2.2 Bandwidth Limitation

System level requirements for EER PA using two-tone signals were discussed in [21]. For a two-tone signal,

$$x(t) = \cos((\omega_c + \frac{\Delta\omega}{2})t) + \cos((\omega_c - \frac{\Delta\omega}{2})t), \tag{4.1}$$

where $\Delta\omega$ is the frequency spacing; the envelope is

$$\left|\cos(\Delta\omega\, t)\right| = \frac{2}{\pi}\left(1 - \sum_{n=1}^{\infty}\frac{2}{4n^2 - 1}\cos(2n\Delta\omega\, t)\right). \tag{4.2}$$

Unlike the original two-tone signal, the envelope signal is not band-limited. To minimize distortion, the supply circuit bandwidth has to be larger than the RF bandwidth. In [21], a supply circuit bandwidth of three times the RF bandwidth is recommended for C/I > 40dBc. The authors in [5] suggest the required supply circuit bandwidths for CDMA and W-CDMA are four times the RF carrier bandwidths. Furthermore, they suggest the supply circuit switching frequency be at least five times the required bandwidth. For W-CDMA applications, the required switching frequency must be over 76.8 MHz, which is very hard to implement efficiently.

Figure 4.3 shows comparison of the envelope spectrums of a 1.92 MHz spaced two-tone signal and a W-CDMA voice signal. From the simulation results, the spectrum of the envelope of a W-CDMA voice signal decays faster than a two-tone signal. It

suggests the required bandwidth of the supply modulator for a W-CDMA EER PA may be less than an EER PA for two-tone signals.

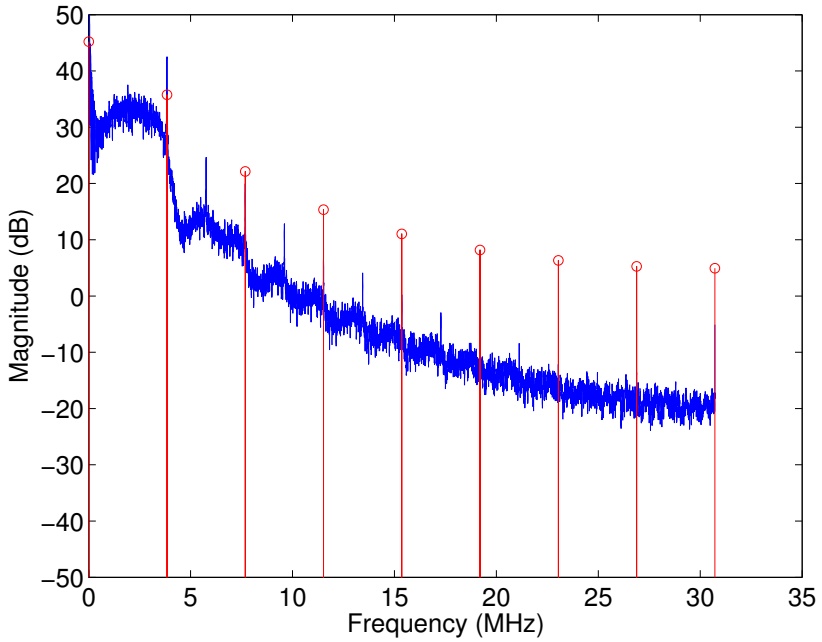


Figure 4.3 Spectrum comparison of two-tone signal (red) and W-CDMA voice signal (blue).

To find the actual bandwidth required for an EER PA for W-CDMA applications. A Kaiser-windowed concatenated sinc function is used to mimic an ideal low-pass filter. The impulse responses of the filters and their frequency responses for various frequencies are shown in Figure 4.4. System-level simulation of an EER PA using W-CDMA voice signal is performed using the aforementioned filter to band-limit the envelope signal. Simulation results using a 121-tap filter is shown in Figure 4.5. A baseband sampling frequency of 61.44 MHz is used. Longer filter lengths, which lead to sharper filter transition, are also used for simulation. However, simulation speed is greatly reduced while showing similar results. From the simulation results, the required envelope path

bandwidth to pass both ACLR specifications is only 5 MHz, which is far lower than the bandwidth suggested in [5].

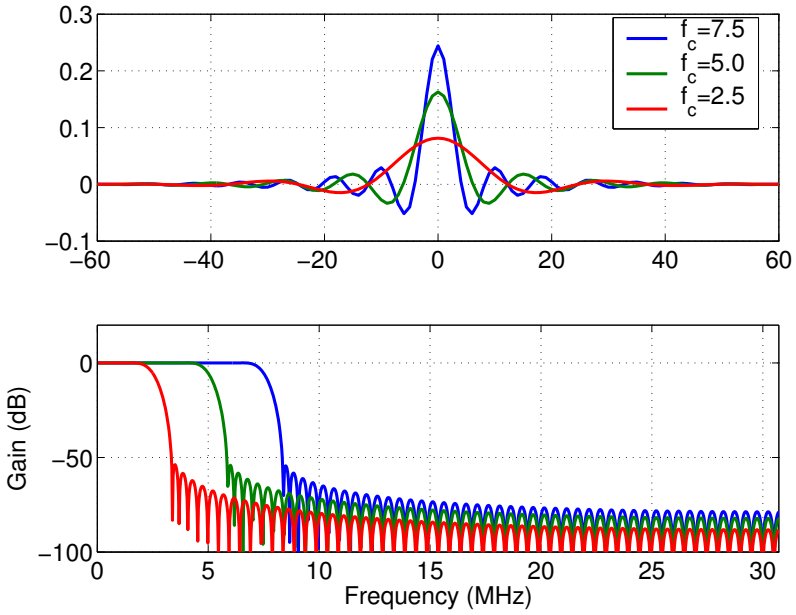


Figure 4.4 Impulse response and frequency response of Kaiser-windowed sinc function used for W-CDMA system simulation.

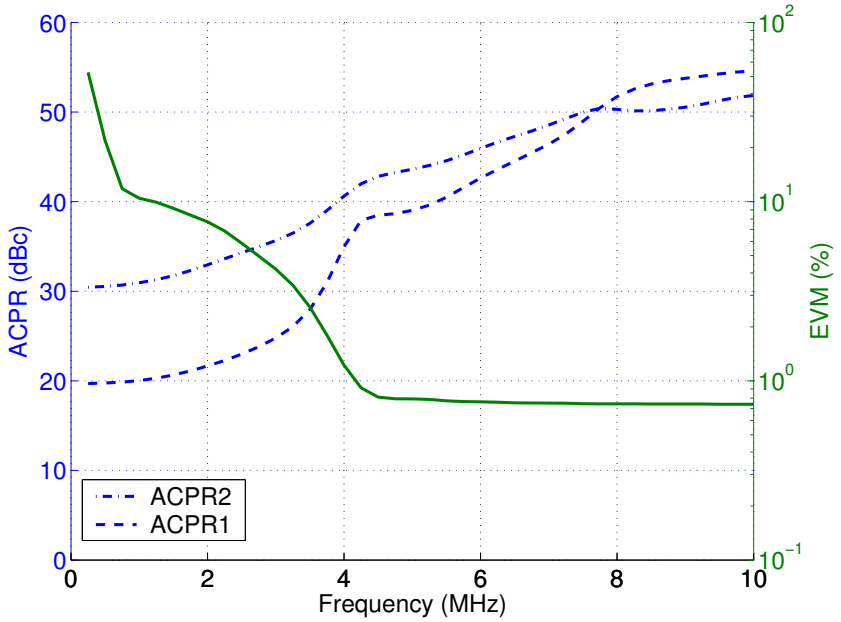


Figure 4.5 System-level simulation results of an EER PA for W-CDMA application.

4.2.3 Delay Mismatch Limitation

The authors of [19] and [21] suggest that the intermodulation distortion of a two tone signal for an EER PA is proportional to the square of the signal spacing and the delay mismatch between the phase signal and the envelope signal. Results of system-level simulation of EER PA using a W-CDMA voice signal for various envelope path bandwidths and delay mismatches are shown in Figure 4.6 and Figure 4.7. The simulation results show that an EER PA can pass both ACLR specifications when the delay mismatch is less than one period of a sampling frequency of 61.44 MHz, which is about 16 ns.

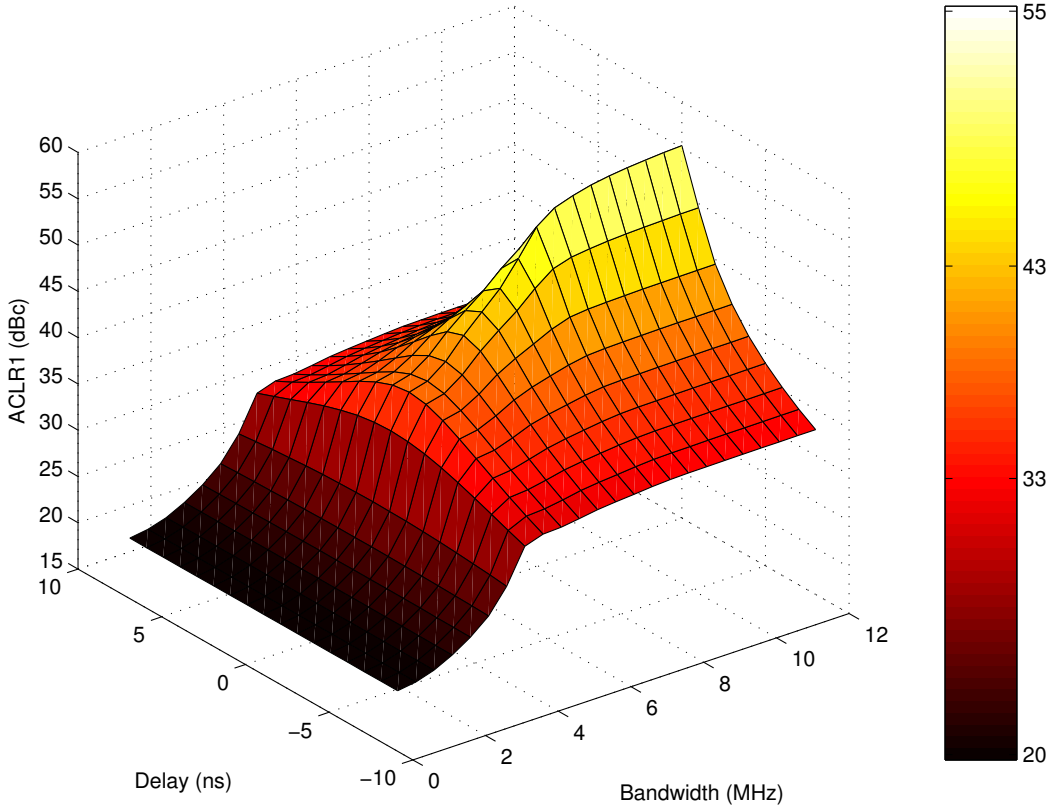


Figure 4.6 Adjacent channel leakage power ratio simulation of an EER PA using a W-CDMA voice signal.

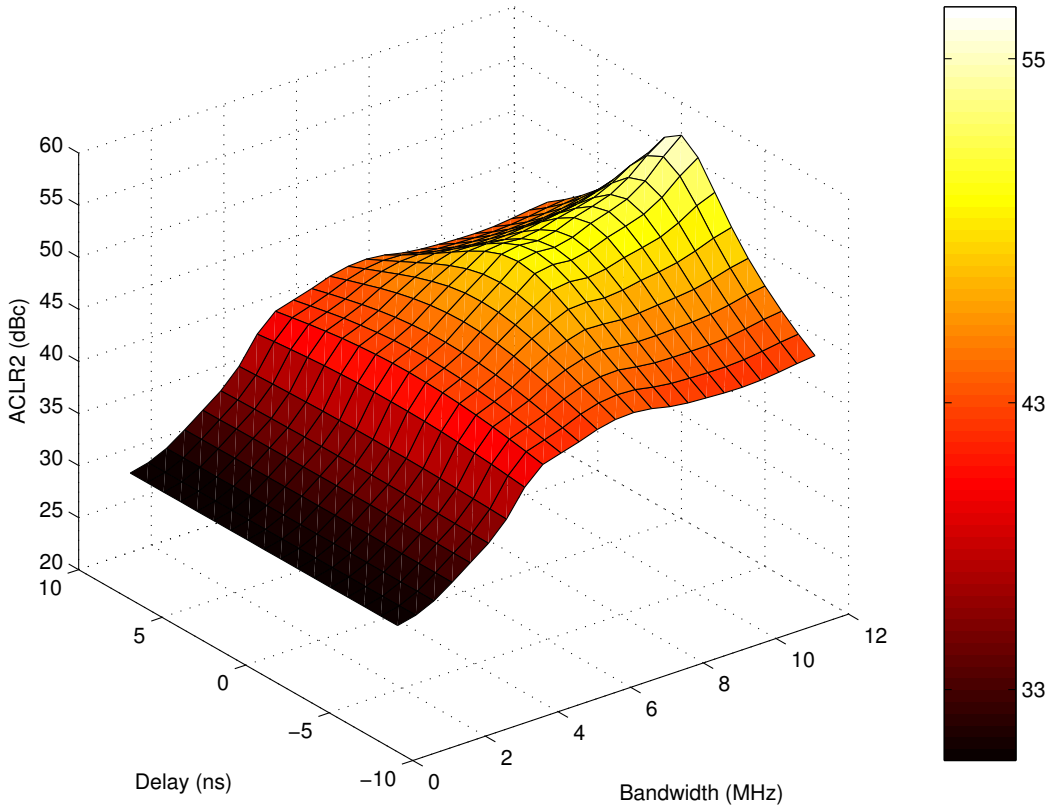


Figure 4.7 Alternate channel leakage power ratio simulation of an EER PA using a W-CDMA voice signal.

4.3 Dual-Phase PWM Supply Circuit

The use of a multi-phase switching regulator is a way to achieve high current output with reduced passive component sizes [39]. The multi-phase switching regulator also has an effective switching frequency that is the number of phases multiplied by the switching frequency of each phase. Because multiple high-efficiency switching regulators with low switching frequency are used, the overall efficiency is higher than a single phase switching regulator with the same bandwidth.

One problem with using switching regulators in dynamic-biased PAs is the size of the off-chip inductor. For a single phase switching regulator, the inductor must be able to

handle the peak current that the PA draws. Inductors with low enough DC resistance and high enough current handling capability are usually too large in size to fit into modern handsets. Because each phase in a multi-phase switching regulator only needs to supply a portion of the maximum output current, smaller-sized inductors with lower current handling capability can be used enabling more compact designs.

In this work, a dual-phase PWM supply circuit is designed using 0603 240 nH RF inductors from Coilcraft. The basic block diagram is shown in Figure 4.8. The supply circuit IC is implemented with AMI 0.6 μm 2P3M CMOS process through MOSIS. The die size is 1.5 mm by 1.5 mm, and the chip is packaged in a Kyocera CLCC28 package. The photo of the test board is shown in Figure 4.9, and the die photo is shown in Figure 4.10.

The off-chip LC filter capacitors are 0402 SMD capacitors. Besides the inductors, all other components for the dynamic supply circuit can be integrated in a single chip. With the use of 0603 inductors, it is also possible to integrate the complete dynamic supply circuit into a PA module. The supply circuit is designed and verified to work from a supply voltage of 2.5 V to 5.0 V. The maximum effective switching frequency is in excess of 100 MHz.

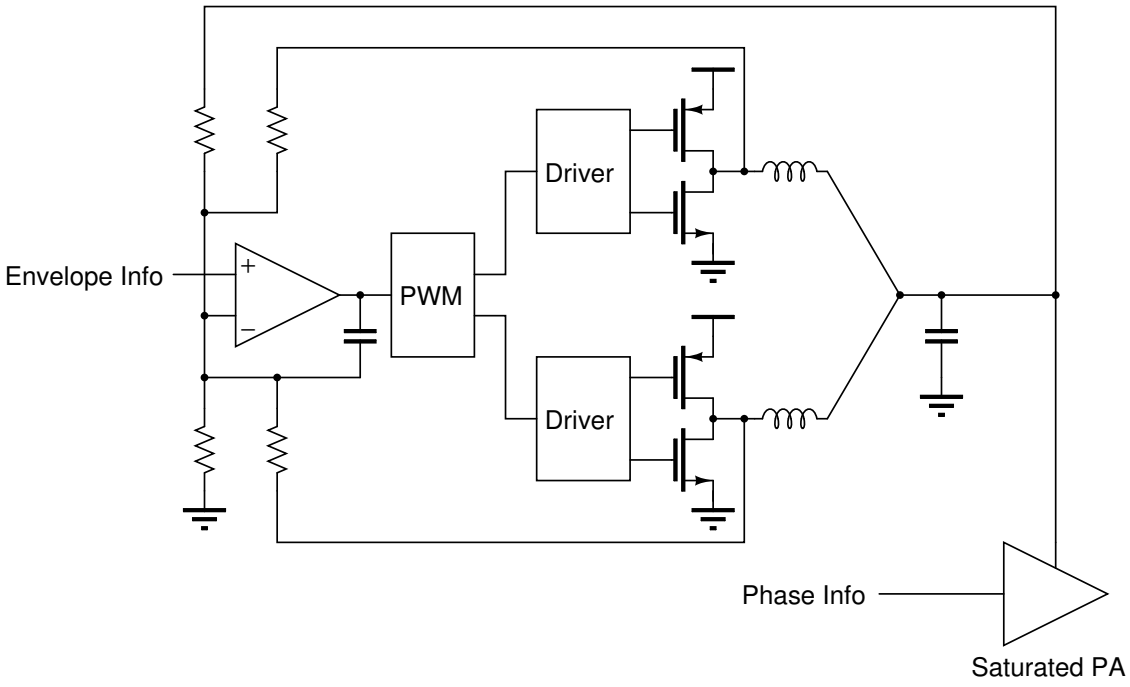


Figure 4.8 Block diagram of EER PA using a dual-phase PWM supply circuit.

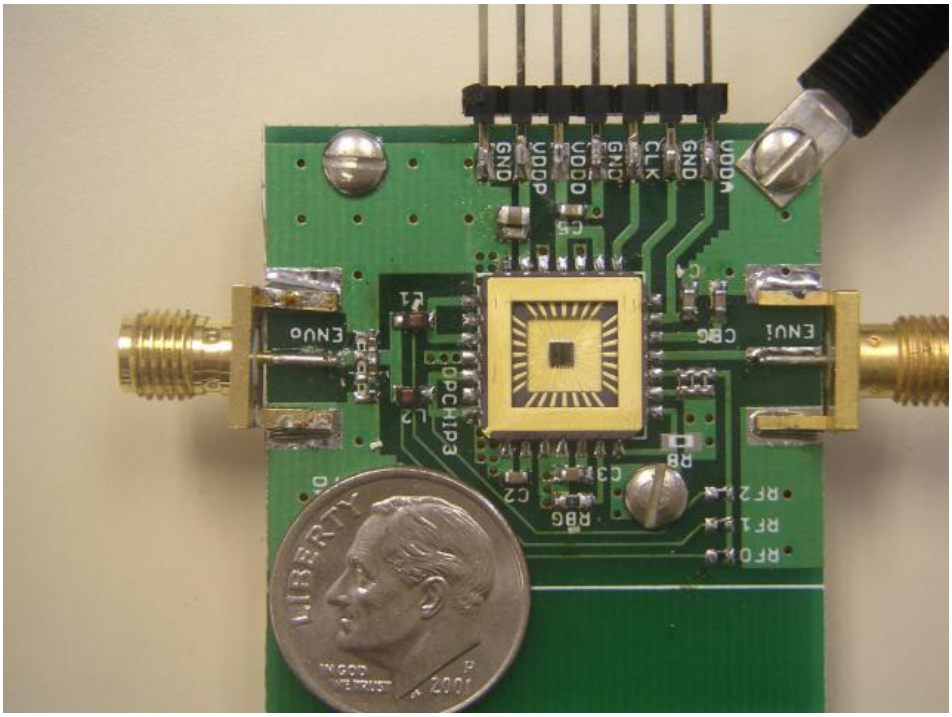


Figure 4.9 Photo of test board for dual-phase PWM supply circuit.

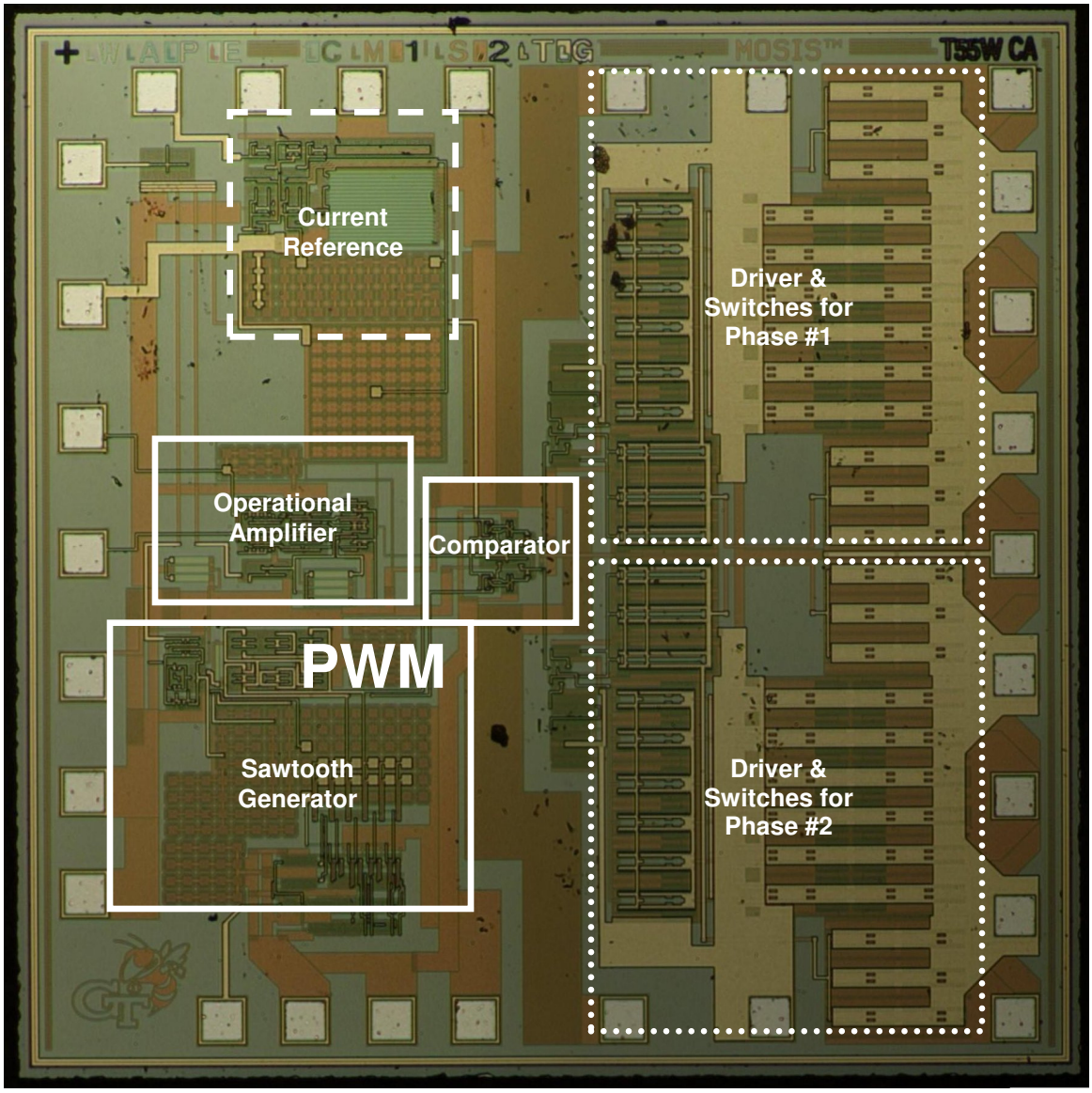


Figure 4.10 Die photo of dual-phase PWM supply circuit.

4.4 RF PA Characterization for EER PA

Polar transmitters and EER PAs reported in the previous literature are all closed-loop implementations [26-28]. To achieve the required flat gain bandwidth and group delay, dynamic supply circuits with bandwidths of several times the channel bandwidth were required. Those implementations have been limited to low bandwidth applications such as NADC with 30 kHz bandwidth and EDGE with 200 KHz bandwidth. For the 3.84 MHz bandwidth W-CDMA standard, such conservative design practices become unrealistic.

The implementation of a full closed-loop polar transmitter requires an additional receiver or a linear detector used for correction. For stability, the overall bandwidth is often a small fraction of the switching frequency. To achieve higher bandwidth, an open-loop architecture is used, but such an architecture requires accurate characterization of the RF PA. This section shows the detailed characterization of the Sirenza SHF-0289 RF PA used in this work.

4.4.1 Amplitude and Phase Characterization

In the implementation of an EER PA, the RF PA is driven by a constant envelope signal. The output RF power is solely controlled by the drain or collector voltage supplied by the dynamic supply circuit. By using a single-tone signal with varying drain or collector voltage, the amplitude response of the EER PA can be characterized. By comparing the phases of the input and output single-tone signal of the RF PA, the phase response can also be characterized. The characterization setup is shown in Figure 4.11. The baseband arbitrary waveform generator of an Agilent ESG 4432B is used to generate

a reference voltage. Since the reference voltage can only be between 0 V and 1 V, a preamplifier is used to amplify the voltage to drive the dynamic supply circuit.

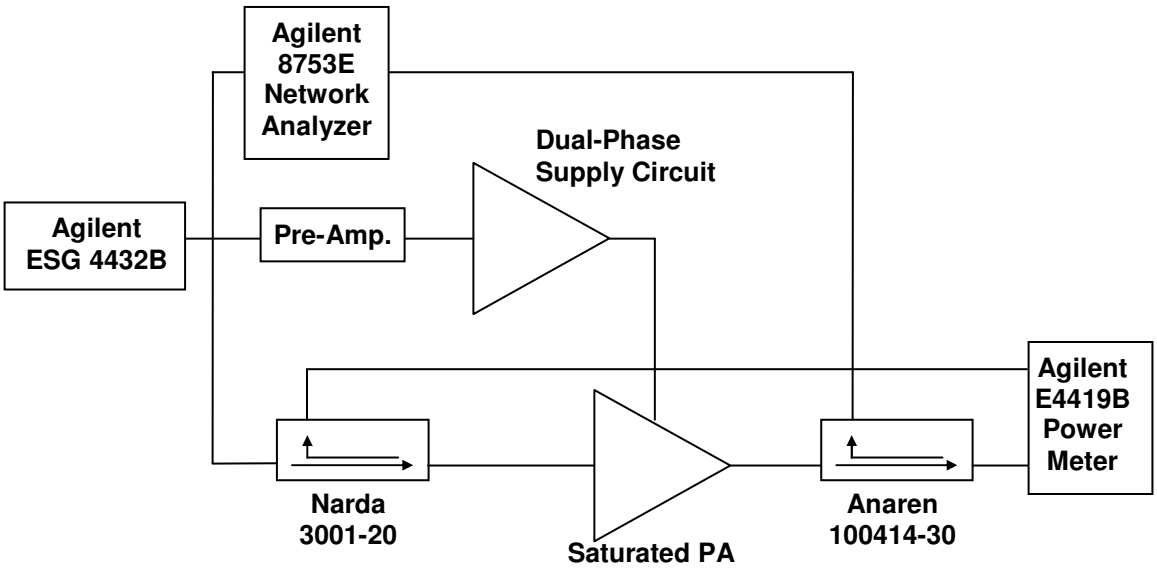
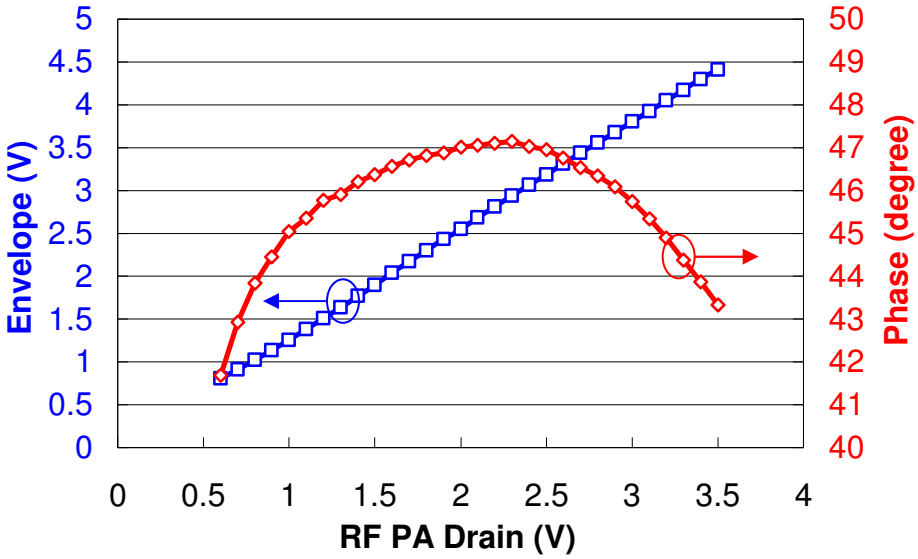


Figure 4.11 RF PA characterization setup.

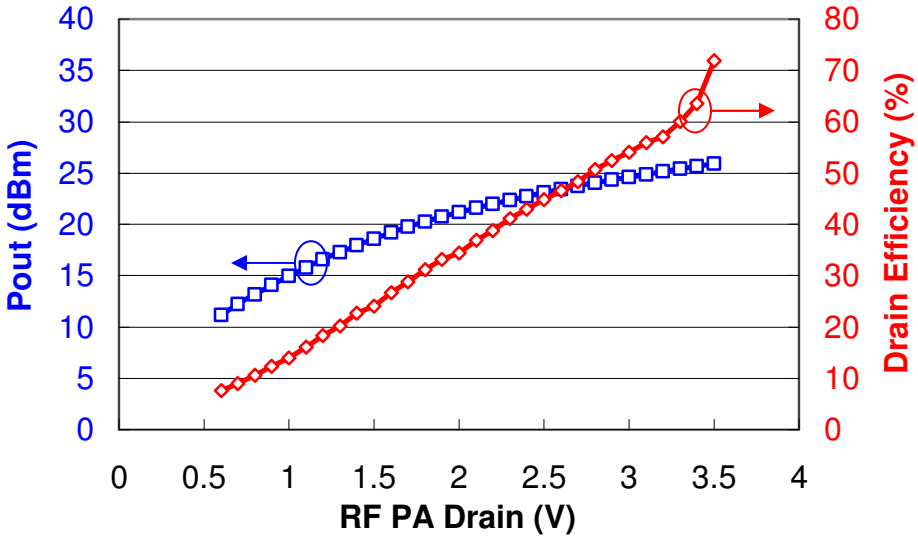
The input RF power level and the RF PA gate voltage are swept. An input power level of 11.5 dBm and a PA gate bias of -0.8 V were chosen for low phase distortion. Amplitude (envelope) and phase characterization results are shown in Figure 4.12(a). The output power and drain efficiency versus PA drain voltage are shown in Figure 4.12(b).

With the characterization data, the relationship between the output envelope voltage and the RF PA drain voltage can be found. Using the previously derived function, the baseband envelope signal can be scaled according to the desired output power level and fed into the dynamic supply circuit. Using a W-CDMA voice signal, the AM-AM and AM-PM characterization can be performed. The characterization setup is shown in Figure 4.13. The RF signal is down-converted and digitized with a Gage Compuscope

14100 ADC board. The digitized signal is demodulated and processed in Matlab. The measurement results are shown in Figure 4.14.



(a) Amplitude and Phase Characterization



(b) Output power and drain efficiency

Figure 4.12 RF PA characterization results.

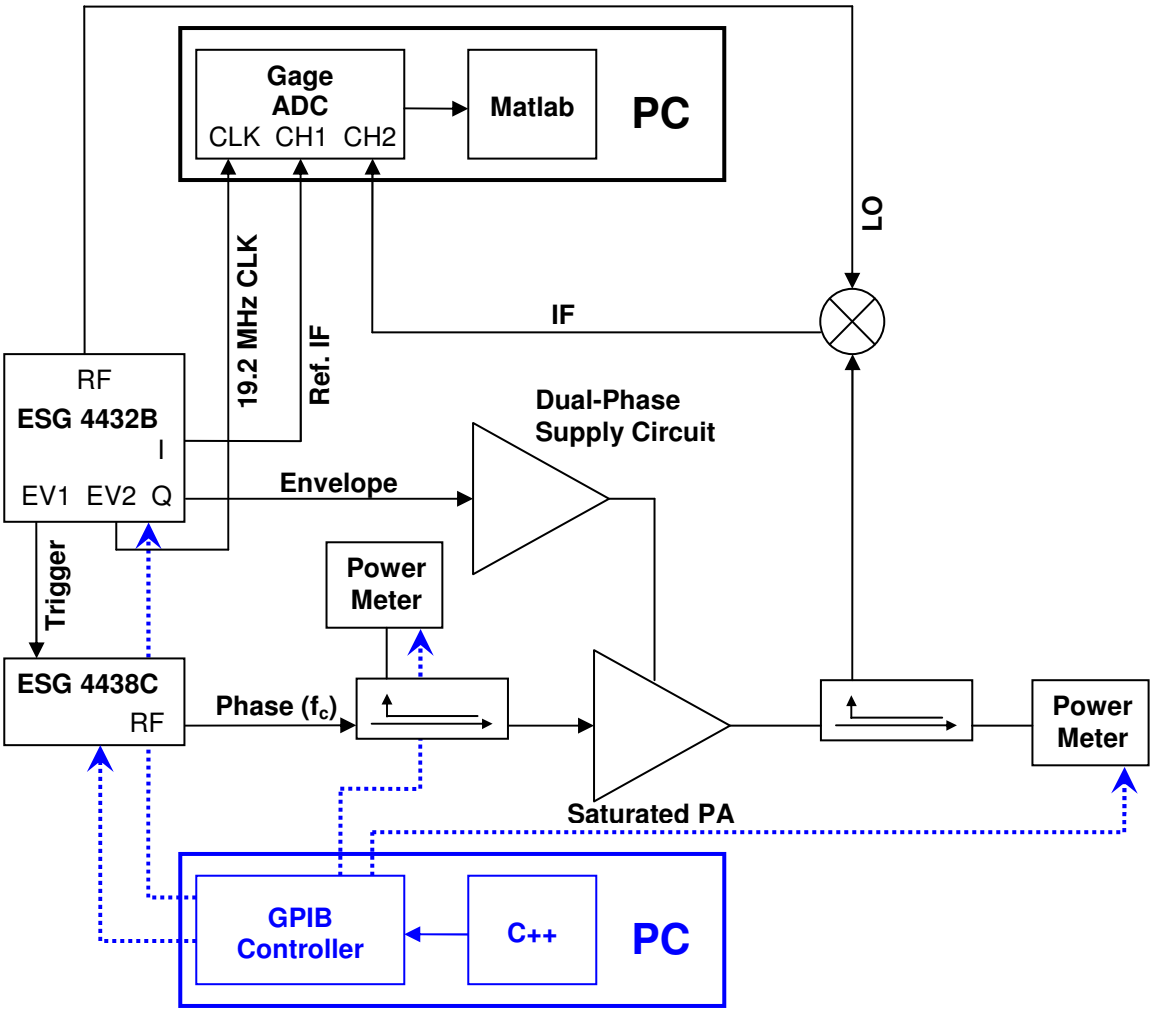
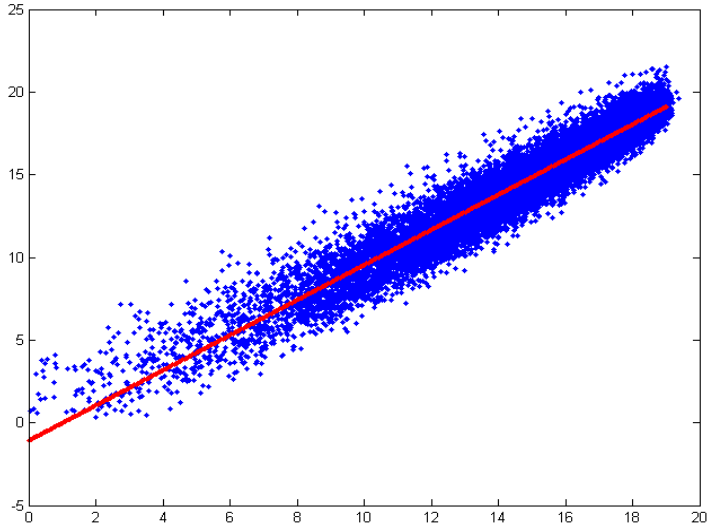
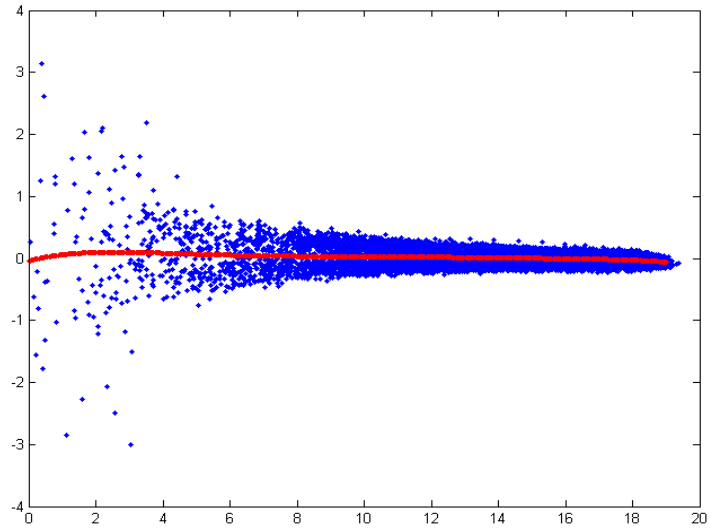


Figure 4.13 AM-AM, AM-PM, and EVM measurement setup.



(a) AM-AM



(b) AM-PM

Figure 4.14 AM-AM and AM-PM characterization results.

From the AM-AM and AM-PM characterization results, the output has large variations for any specific input power level. However, the curve-fitted results match well with the data shown in Figure 4.12(a). The time domain demodulated signal is compared with the input reference signal and shown in Figure 4.15. The two signals match fairly well except at peaks with RMS error of around 8%. Such results suggest the

characterization of the RF PA with DC voltages is not sufficient. The next section proposes an improved characterization technique.

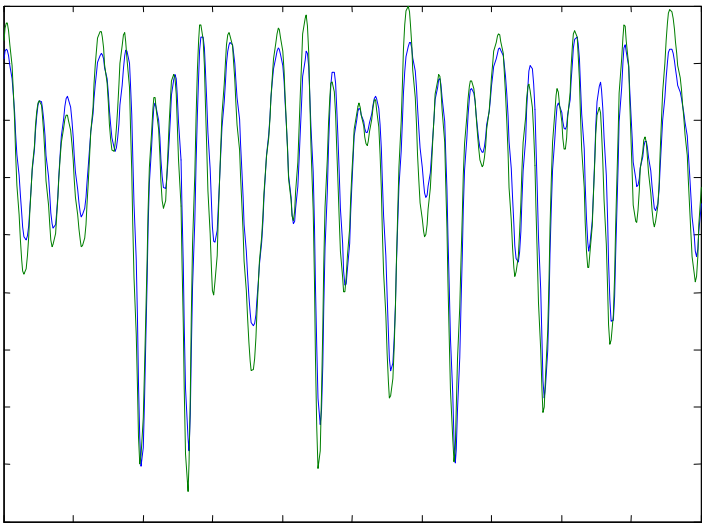


Figure 4.15 Time domain comparison of demodulated signal and reference signal.

4.4.2 Frequency Response Characterization

The characterization results in 4.2.1 show that the use of a DC voltage to characterize the RF PA is not satisfactory. Characterization of the dynamic supply frequency response is also necessary. Characterization of the EER PA is usually done with two-tone signals as in [21]. However, the envelope of a two-tone signal, as shown in (4.2), is not band limited and can not accurately characterize the frequency response of a dynamic supply circuit, or an envelope amplifier. An envelope signal composed of a single frequency has the form of $1+a\cos(\omega_{env}t)$, where a is a constant and $a \leq 1$ so the envelope is never negative. When characterizing, a sinusoidal waveform, $\cos(\omega_c t)$ is used as the RF PA input. With the EER PA operating as a multiplier, the output RF signal is a three-tone signal with the form of

$$v_{out}(t) = \cos(\omega_c t) + \frac{a}{2}\cos((\omega_c - \omega_{env})t) + \frac{a}{2}\cos((\omega_c + \omega_{env})t). \quad (4.3)$$

Using this signal, the frequency response of an EER PA can be accurately characterized.

The measurement setup for frequency response characterization of the dynamic supply circuit is shown in Figure 4.16. An S21 measurement is performed before and after the dynamic supply circuit and shown in Figure 4.17 and 4.18, respectively. By dividing the two measurement results, the effect of the bias-tee and preamplifier can be removed and the frequency response of the dynamic supply circuit can be obtained. From the phase response of the dynamic supply circuit, the group delay of the bias circuit is calculated and shown in Figure 4.19. The group delay of the bias circuit can be used to determine the delay compensation needed to synchronize the envelope signal and phase signal. Group delay measurements are noisy because of aliasing caused by insufficient filtering at high frequency, which is further amplified after differentiation of the phase measurement data.

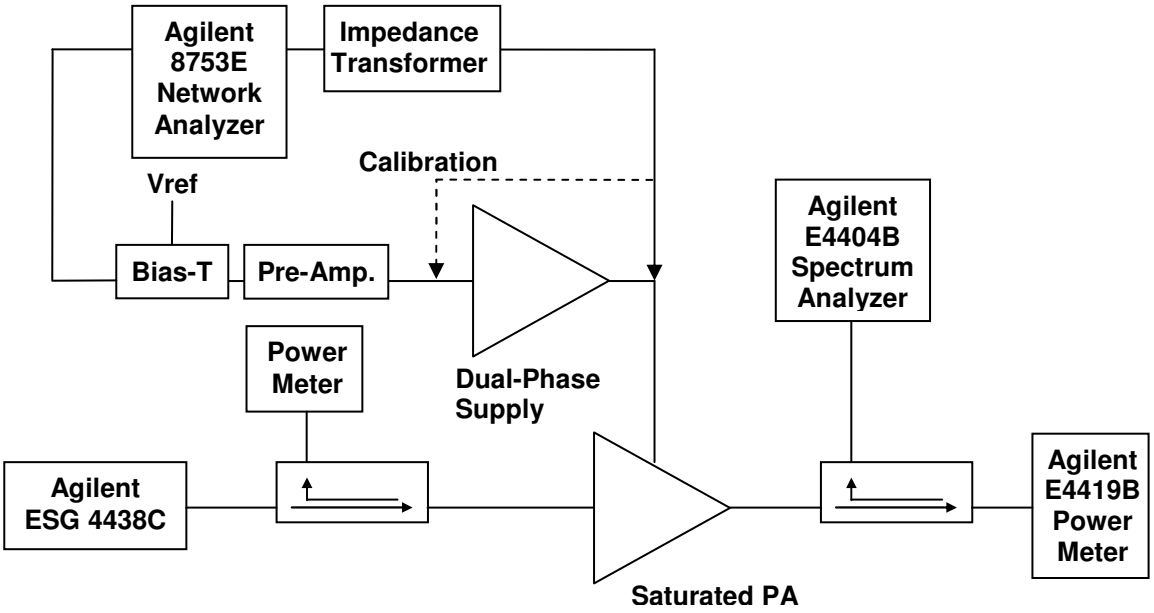


Figure 4.16 Measurement setup for frequency response characterization.

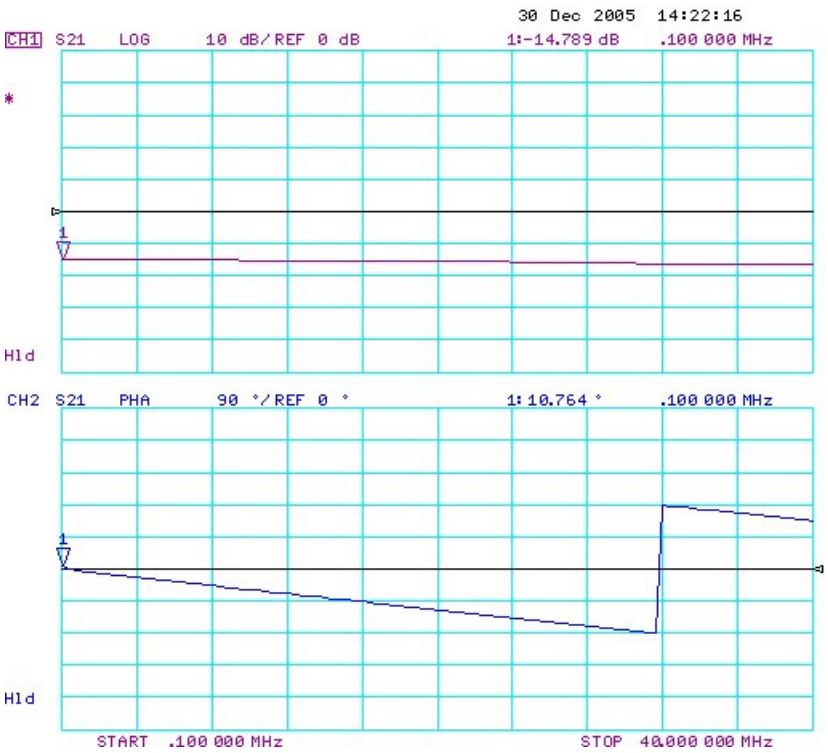


Figure 4.17 Gain and phase response of measurement setup for calibration.

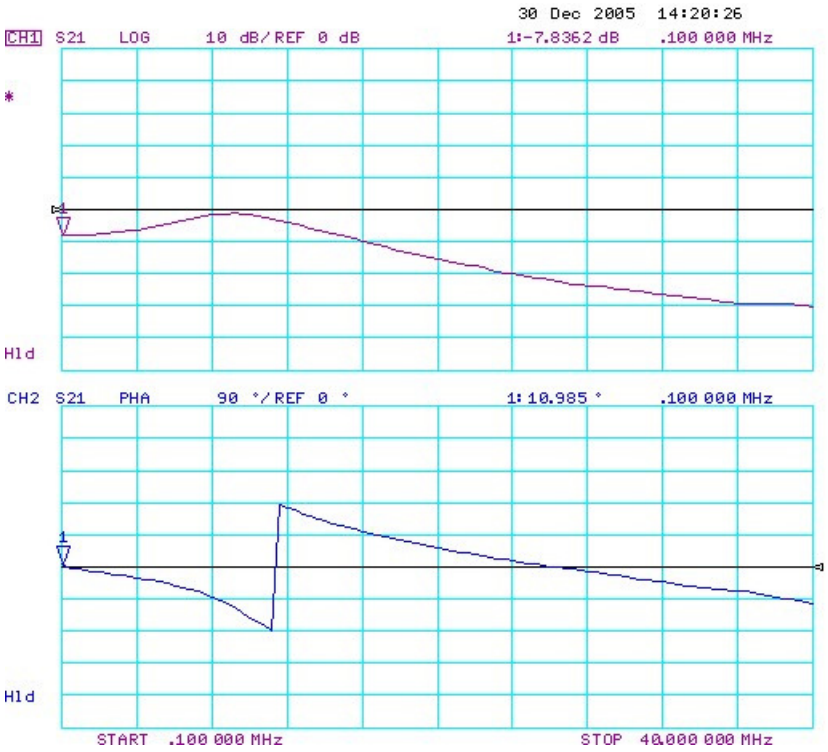


Figure 4.18 Uncalibrated gain and phase response of circuit.

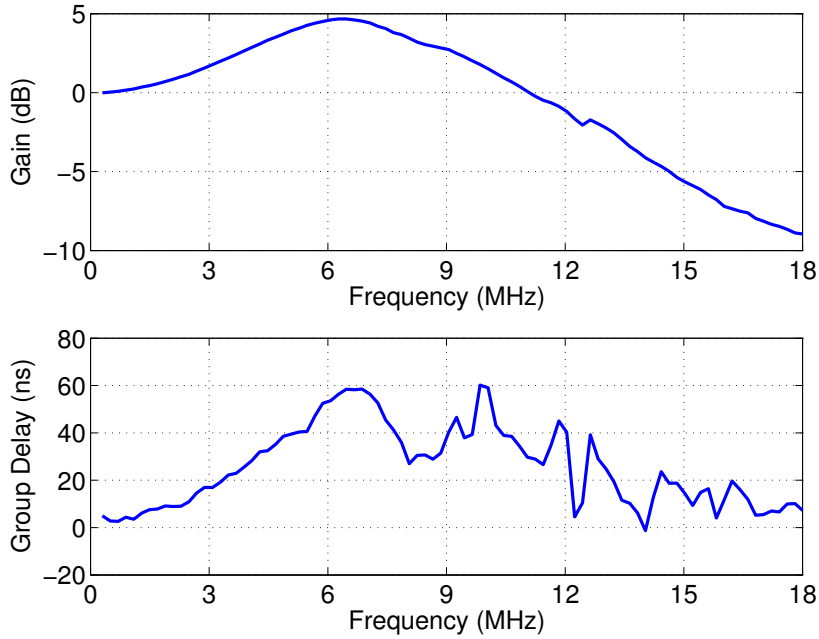


Figure 4.19 Calibrated gain and group delay of dynamic supply circuit.

4.5 Gain Compensation Using Digital FIR Filter

The measurement results in Figure 4.19 show frequency dependent gain and group delay variation within the envelope bandwidth. To compensate for the gain variations in the LC filter in the envelope path while maintaining low group delay variation, a linear phase 121-tap FIR filter was designed and inserted in the envelope path prior to digital-to-analog conversion. A FIR filter tap weights were set to achieve a magnitude response that approximates the reciprocal of the amplitude response of the converter and filter. The frequency response was compensated up to about 12 MHz. The simulated frequency response of the compensation filter is shown in Figure 4.20, along with the overall frequency response of envelope path. It is seen that the amplitude response is flat to within ±0.5 dB up to 12 MHz. The digital FIR filter has a constant group delay that must be compensated for by inserting a constant digital delay in the

phase path before it is converted to analog form. This is simply added to the delay that must already be used to offset the group delay in the PWM and passive LC filter. The block diagram of the overall polar transmitter system implementation is shown in Fig. 4.21.

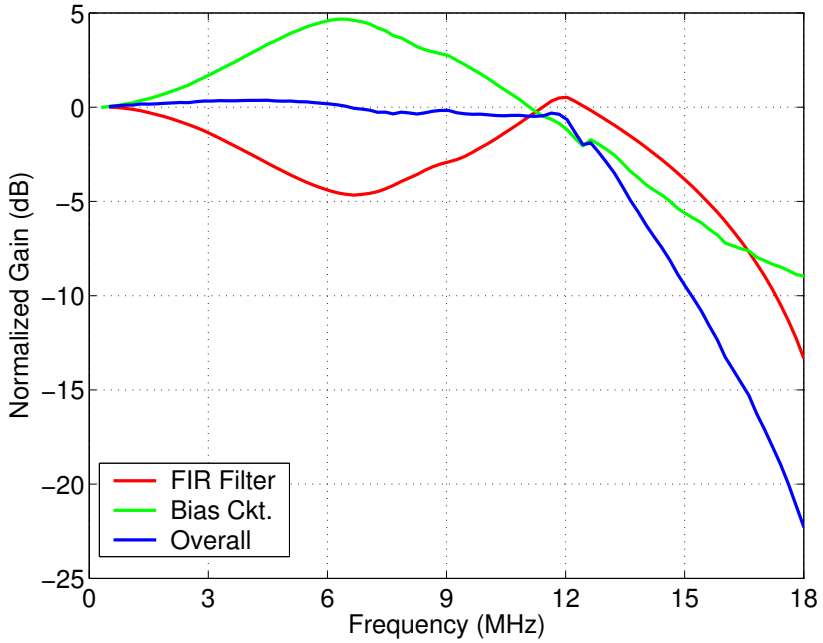


Figure 4.20 Simulated frequency response of envelope amplifier and bias circuit, gain compensation FIR filter, and overall response of both combined.

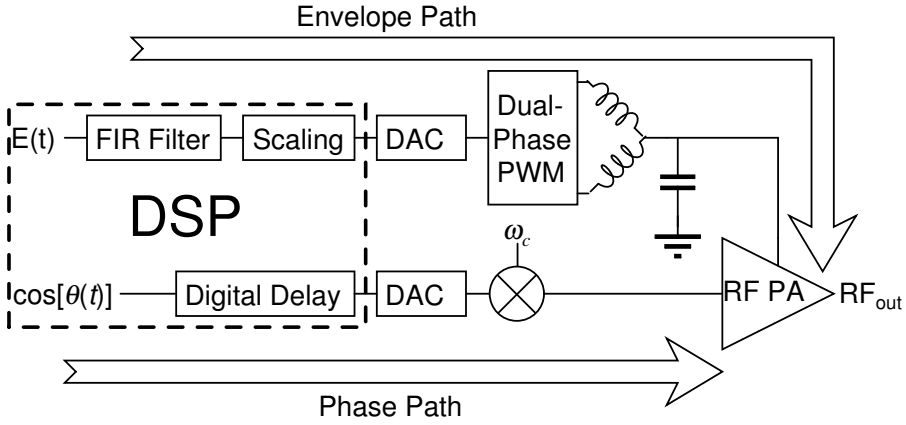


Figure 4.21 Block diagram of the EER PA system with gain compensation.

An 836.5 MHz W-CDMA voice signal is used to test the implemented polar transmitter system. The waveform is processed in a C++ program to implement the envelope gain compensation and phase path delay compensation, and subsequently loaded into an Agilent E4432B signal generator to produce the baseband amplitude path signal that was applied to the PWM input. The constant envelope phase modulated signal was loaded into an Agilent E4438C signal generator, and applied to the RF PA input. A 3.5 V input supply voltage is used to characterize the response of the system. To assess the performance of the system for use in cellular phone applications, a W-CDMA carrier with a single voice channel was created. Amplitude and phase signals were extracted and loaded into the signal generators. Drain efficiency and power added efficiency (PAE) for the PA were recorded over a range of input power, and are shown in Fig. 4.22. The ACLR measurement results are shown in Fig. 4.23. By using a gain compensation FIR filter before the supply circuit, ACLR is improved by as much as 10 dB to pass the W-CDMA specifications over a range of transmitted power.

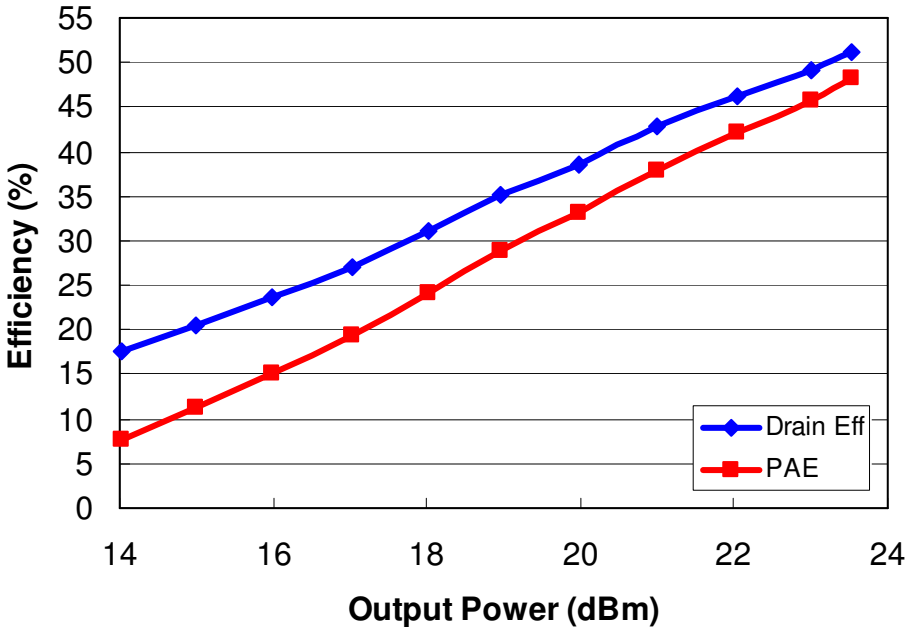


Figure 4.22 Drain efficiency and PAE of the polar transmitter with V_{DD} = 3.5 V using a W-CDMA signal at 836.5 MHz.

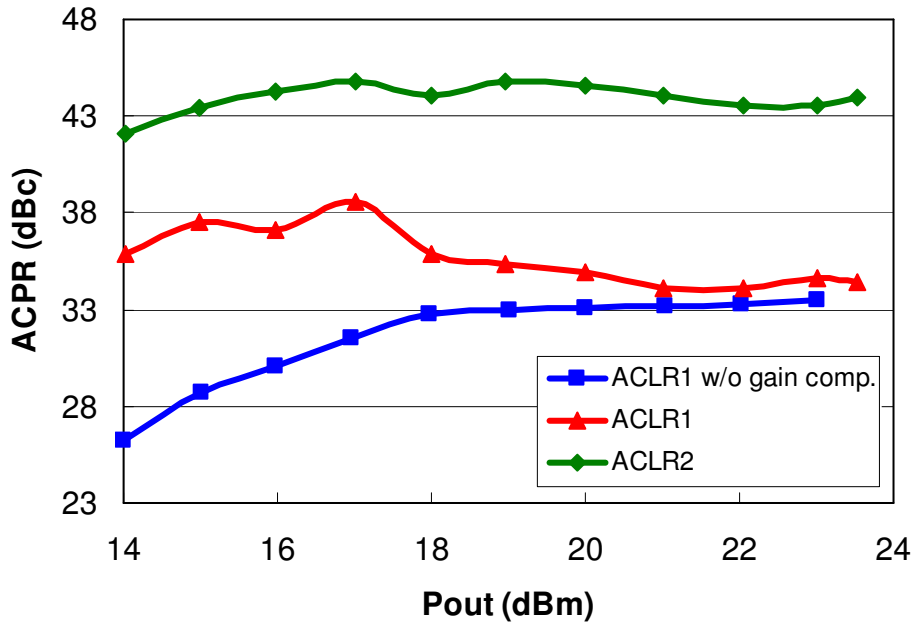


Figure 4.23 Measurement results of ACLR with V_{DD} = 3.5 V using a W-CDMA voice signal at 836.5 MHz.

The CMOS buck converter is designed to operate from a supply voltage of 2.5 V to 5.0 V. Measurements using supply voltages from 2.5 V to 4.5 V were performed and are summarized in Table 4.2. The $P_{o,peak}$ is defined as the maximum output power measured that can pass both ACLR specifications. The measurement results show the robustness of the RF PA characterization over supply variation.

Table 4.3 W-CDMA EER PA Measurement Results for Various Supply Voltages

V_{DD}	$P_{o,peak}$	ACLR1	ACLR2	η_{drain}	PAE
2.5 V	19.7 dBm	34.3 dBc	44.4 dBc	49.3 %	41.8 %
3.0 V	22.2 dBm	35.0 dBc	43.9 dBc	51.3 %	47.0 %
3.5 V	23.5 dBm	34.4 dBc	44.0 dBc	51.3 %	48.1 %
4.0 V	24.6 dBm	34.8 dBc	43.7 dBc	49.5 %	47.1 %
4.5 V	25.9 dBm	33.3 dBc	43.1 dBc	49.0 %	47.2 %

In-band spurious output is a major concern for EER transmitters because of switching noise. Fig. 4.22 shows the wideband spectrum of the polar transmitter at full output power at 3.5V input voltage. It is seen that the 25 MHz spurious signals are fully suppressed by the two-phase PWM. The 50 MHz spurious signals appear about 43 dB down from the carrier. Because these signals are outside of the transmit band, they would effectively suppressed by the duplexer before transmission. For a typical duplexer used in the cellular band, the suppression in the RX band (869 MHz – 894 MHz) is about 45 dB [45]. The worst case scenario in this implementation is at P_{out}=23.5 dBm. With 88 dB of total suppression, the worst case spurious emission in the RX band is -64.5 dBm, which passes the spurious emission specification shown in Table 4.1. Worst-case suppression

for the lower 50 MHz spurious signal occurs when the center frequency is at 846.5 MHz. For a typical cellular band duplexer as in [45], the suppression of the lower 50 MHz spurious signal is always greater than 8 dB, which easily passes the spurious emission specification [53].

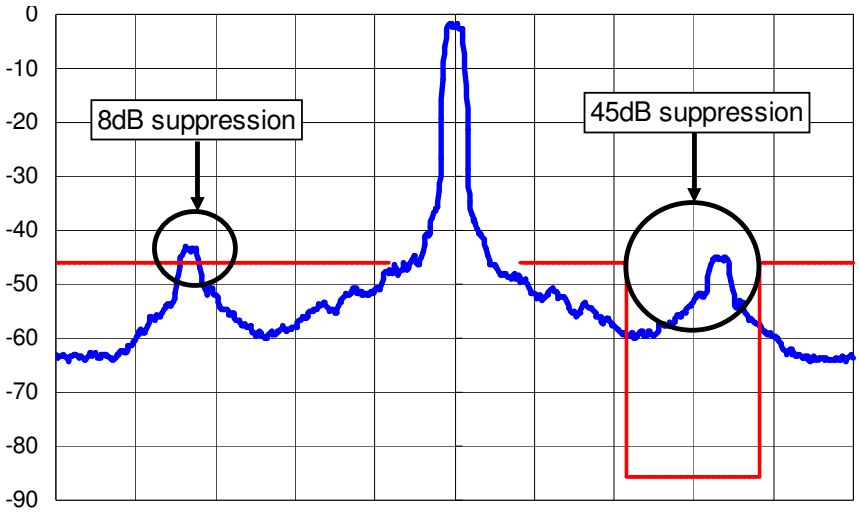


Figure 4.24 Measured wideband spectrum of the EER PA (blue) at 23.5 dBm P_{out} and spurious emission requirements for W-CDMA band V transmitter (red). Center frequency: 836.5 MHz, span: 150 MHz.

4.6 Crest Factor Reduction for Polar Modulation

Pulse shaping is used to limit the occupied bandwidth of digital data while transmitting and thus increasing spectral efficiency. However, the trade-off of limiting bandwidth is increased amplitude variation, as shown in Figure 4.25, where a digital pulse train is shaped with a raised cosine filter. Figure 4.26 shows the constellation of a QPSK signal pulse-shaped with a raised cosine filter. After pulse shaping, the peak amplitude is greatly increased and it is the main source of high PAR or crest factor of digitally modulated signals. The high PAR poses the main difficulty in designing PAs

requiring the PAs to be backed-off by the PAR, which leads to lower efficiency. It can be seen that local peaks in Figure 4.25 and Figure 4.26 often do not occur at the original data point. It is desirable to reduce amplitude of the local peaks while preserving the amplitude of the original data point and bandwidth of the signal.

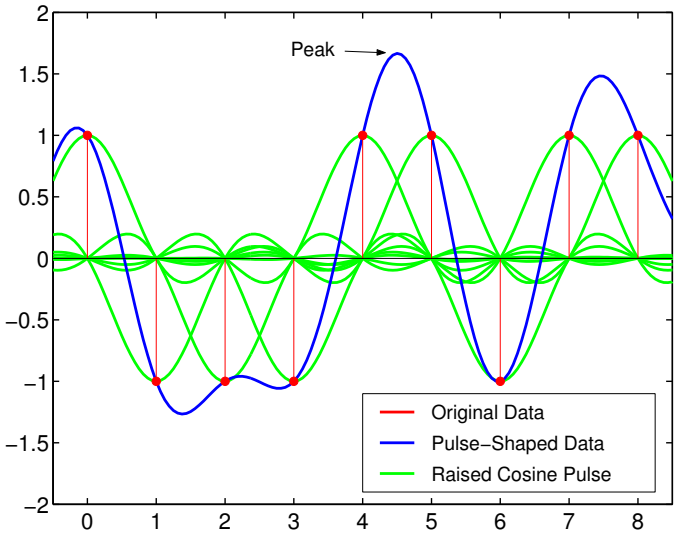


Figure 4.25 Binary data pulse-shaped with raised cosine filter.

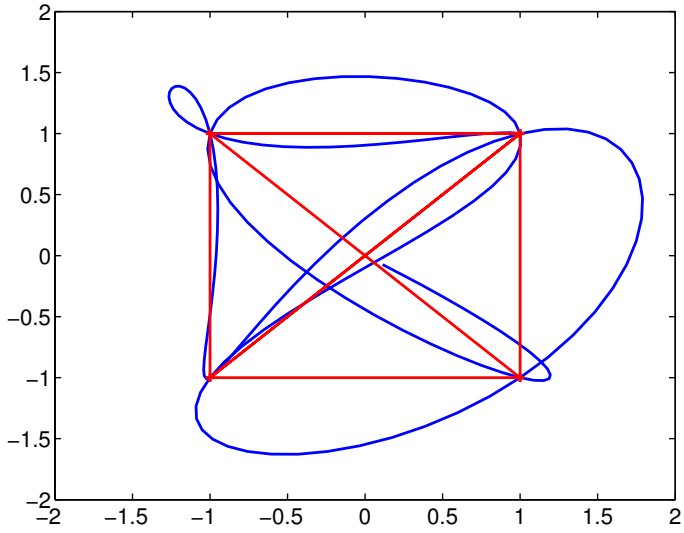


Figure 4.26 Constellation of QPSK signal pulse-shaped with raised cosine filter.

Various methods of CFR are discussed in [40-42] and their references. However, those methods have focused on quadrature modulation. For EER PAs and polar transmitters, where the signals are in polar format, it is unattractive to convert the signals to IQ format for CFR. This section focuses on CFR using polar format signals.

4.6.1 Crest Factor Reduction Using Hard-Clipping

For a signal in polar format, the signal composed of separate amplitude and phase signals. The high crest factor is a result of the peaks in the amplitude data. By clipping the amplitude data, the crest factor can be reduced. The clipping of the amplitude data increases the occupied bandwidth of the original band-limited signal. Since it is not easy to perform digital filtering on polar signals, such implementation seems unattractive. For ease of implementation, digital filtering is performed only on the envelope data. The simulation results for various cut-off frequencies using an FIR filter length of 21 are shown in Figure 4.27. The length of the FIR filter is directly proportional to the power consumption. The simulation results for various FIR filter lengths using a cut-off frequency of 15 MHz are shown in Figure 4.28. For all cases, the EVM is well below the 17.5% requirement specified in the W-CDMA standard. To save computational power, the FIR filter used for CFR can be combined with the envelope path equalization FIR filter.

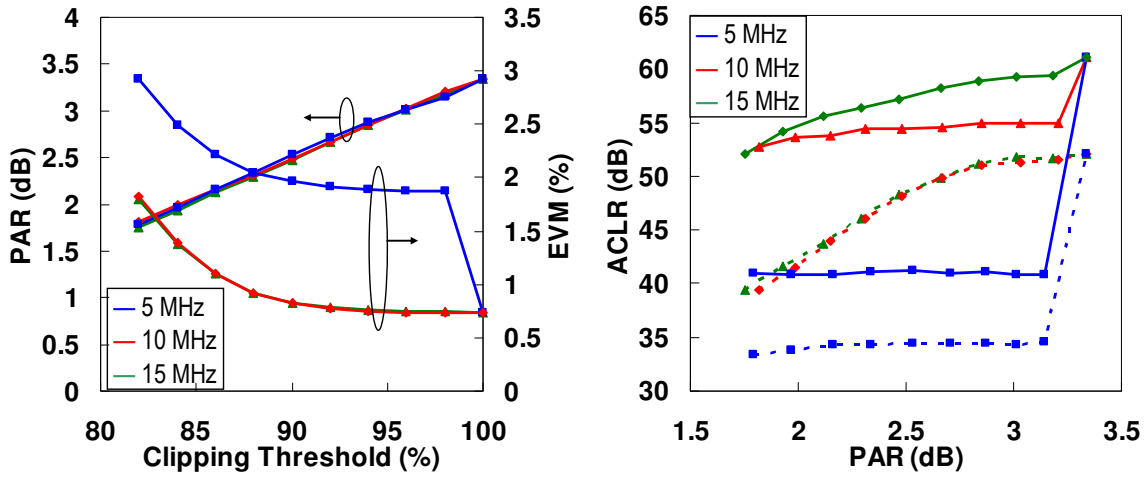


Figure 4.27 System-level simulation of CFR using hard-clipping and digital filtering with various cut-off frequencies for W-CDMA.

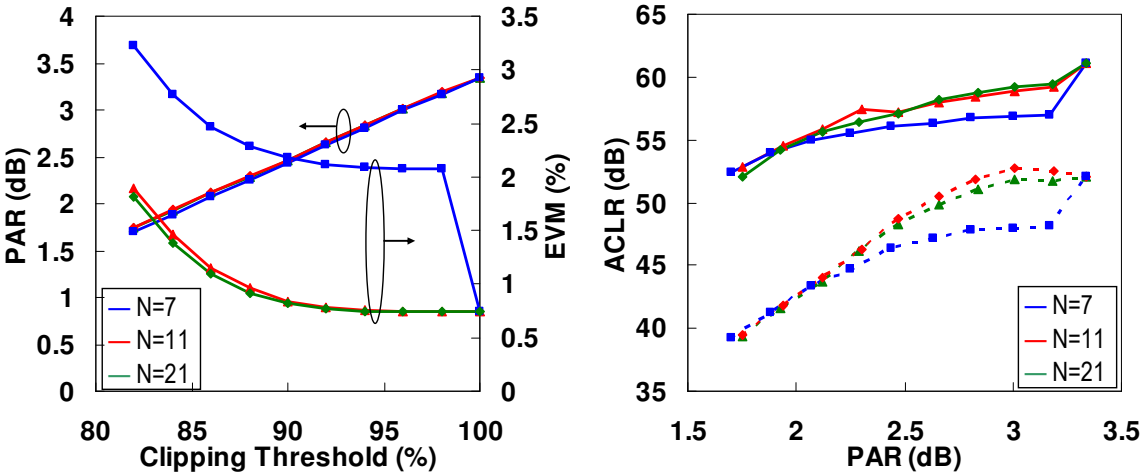
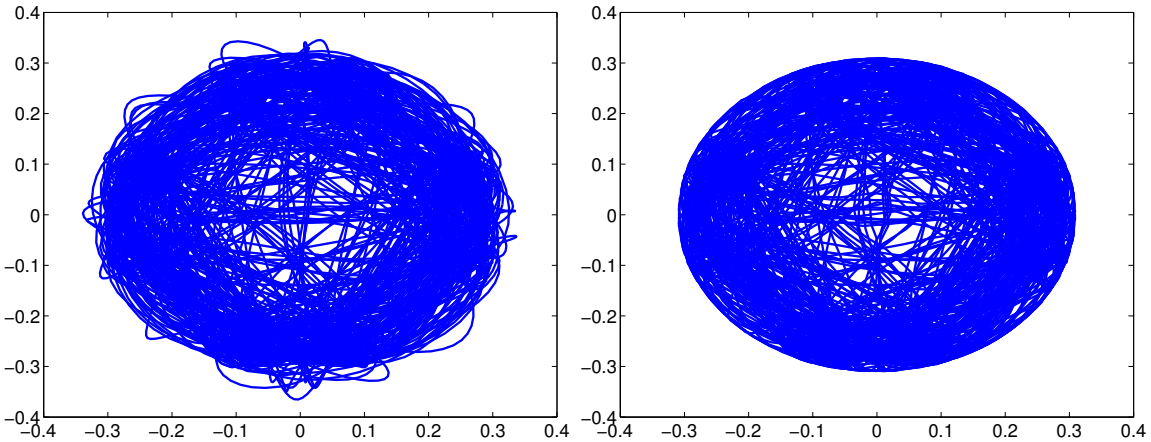


Figure 4.28 System-level simulation of CFR using hard-clipping and digital filtering with various filter lengths for W-CDMA

These system-level simulations using Matlab show the validity of performing digital filtering on only the envelope data and neglecting the phase information is valid. Such implementation uses half the computation power compared to CFR implemented for quadrature modulation. Figure 4.29 shows the effect of CFR to the W-CDMA baseband signal using a clipping threshold of 84% the peak magnitude and a filter length

of 11. The envelope signals and CCDF before and after CFR are compared in Figure 4.30 and Figure 4.31, respectively.



(a) Before CFR (b) After CFR

Figure 4.29 Single voice channel W-CDMA baseband signal before and after CFR using filtering and hard-clipping.

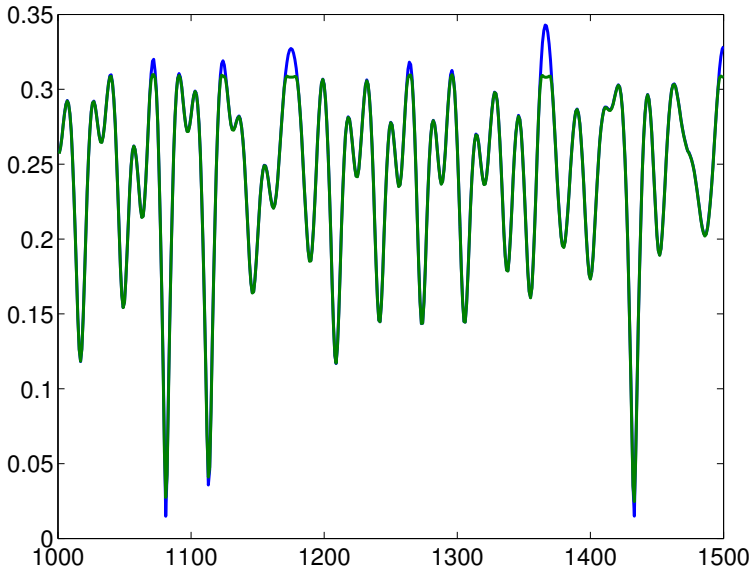


Figure 4.30 Envelope of single voice channel W-CDMA signal before and after CFR using filtering and hard-clipping.

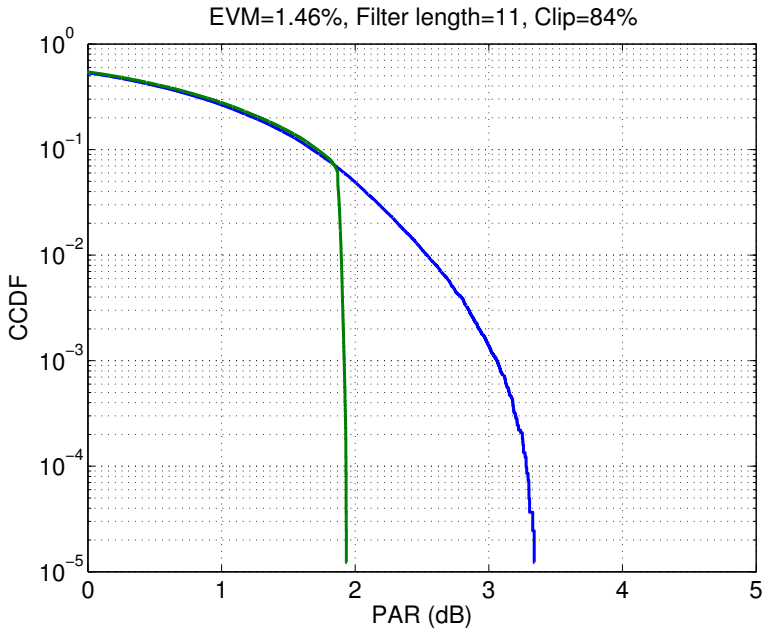


Figure 4.31 CCDF of single voice channel W-CDMA signal before and after CFR using filtering and hard-clipping.

4.6.2 Crest Factor Reduction Using Soft-Clipping

In this work, soft-clipping by adding or subtracting band-limited signal is used as in [41]. A Kaiser-windowed sinc function is used for the implementation. Compared to hard-clipping, soft-clipping does not require actual filtering for the processed signal, which results in lower power consumption.

Using a filter length of 21 and bandwidths of 1.92 MHz and 3.84 MHz, performance of CFR is shown in Figure 4.32. Comparing Figure 4.27 and Figure 4.32, one can see that the EVM is slightly worse for soft-clipping. However, it is still substantially lower than the 17.5% W-CDMA specification. The comparison also shows the maximum reduction of crest factor is about 0.5 dB lower using soft-clipping technique. Using a filter bandwidth of 1.92 MHz, performance of CFR using various filter lengths are compared and shown in Figure 4.33.

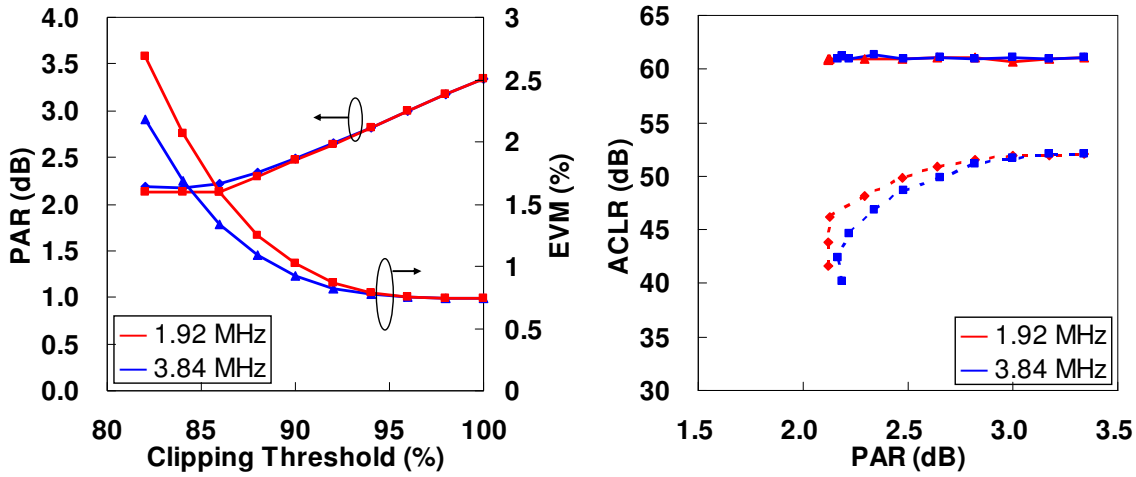


Figure 4.32 System-level simulation of CFR using subtraction of Kaiser-windowed sinc function with various cut-off frequencies for W-CDMA.

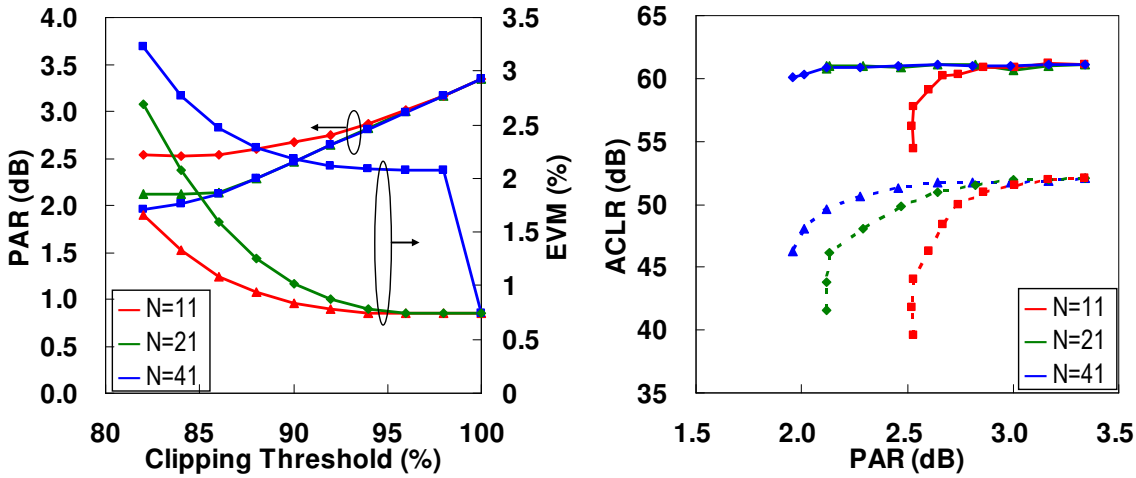


Figure 4.33 System-level simulation of CFR using subtraction of Kaiser-windowed sinc function with various filter lengths for W-CDMA.

The envelope of a W-CDMA voice signal before and after CFR is shown in Figure 4.34. The clipping threshold is 84% of the peak magnitude and the filter length used is 21 with a filter bandwidth of 1.92 MHz. The CCDF of the signal before and after CFR are compared in Figure 4.35.

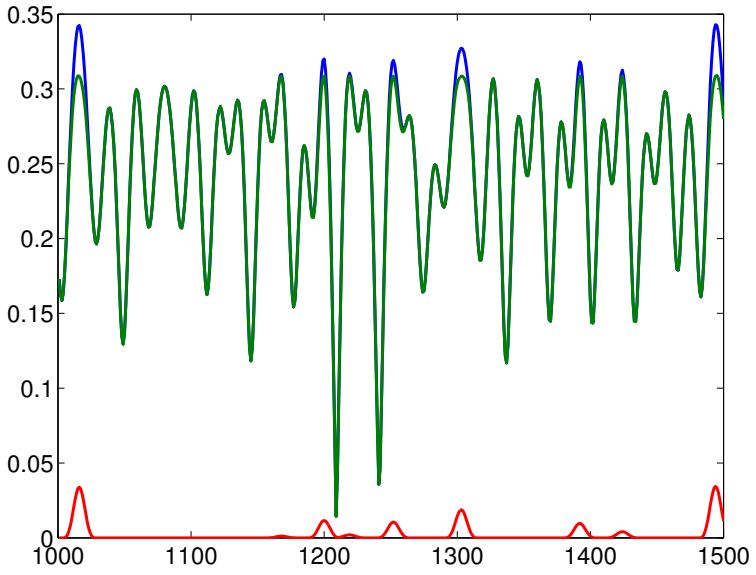


Figure 4.34 Envelope of single voice channel W-CDMA signal before and after CFR using subtraction of Kaiser-windowed sinc function.

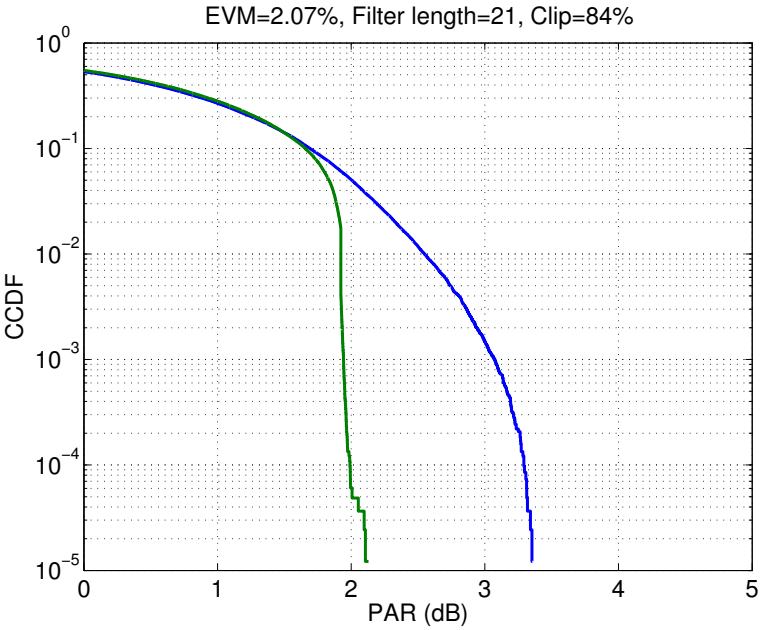


Figure 4.35 CCDF of single voice channel W-CDMA signal before and after CFR using subtraction of Kaiser-windowed sinc function.

To evaluate the performance of CFR with an EER PA, measurements of efficiency and ACLR were performed. The drain efficiency and PAE are compared in

Figure 4.36. The results of the ACLR measurements are shown in Figure 4.37. The EER PA possesses a dynamic range of over 8 dB passing both ACLR requirements for W-CDMA. The maximum measured power that passes the W-CDMA specification is 24.3 dBm, which is 0.8 dB higher than the EER PA without using CFR.

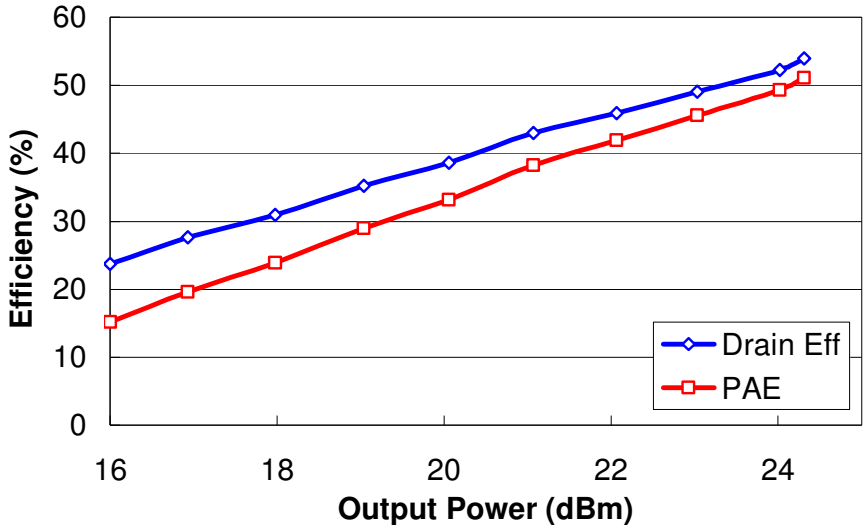


Figure 4.36 Drain efficiency and PAE of the polar transmitter with V_{DD} = 3.5 V using a W-CDMA signal with CFR at 836.5 MHz (PAR = 2.12 dB).

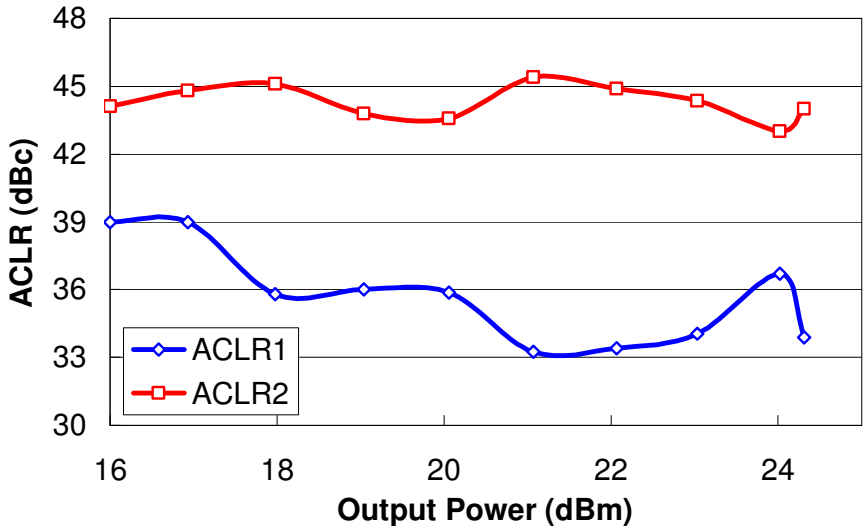


Figure 4.37 Measurement results of ACLR with V_{DD} = 3.5 V using a W-CDMA voice signal with CFR at 836.5 MHz.

Comparing the peak output power level for the EER PA with CFR and without CFR, the difference is only 0.8 dB, which is lower than the reduced PAR, 1.26 dB. Such difference is the result of hard clipping at the peak output power level without using CFR. Slight hard clipping does not create enough distortion for the EER PA to fail the ACLR specifications.

The efficiency of the EER PA with and without CFR is compared for various output power levels and shown in Figure 4.38. The efficiency curves of both methods match fairly well form 14 dBm to 23.5 dBm. From the measurement results, CFR does not improve the efficiency for a specific power level. However, CFR increases the peak output power and peak efficiency. The performance of the EER PA with and without CFR are summarized and compared with other recent-reported wide-band EER PAs in Table 4.4.

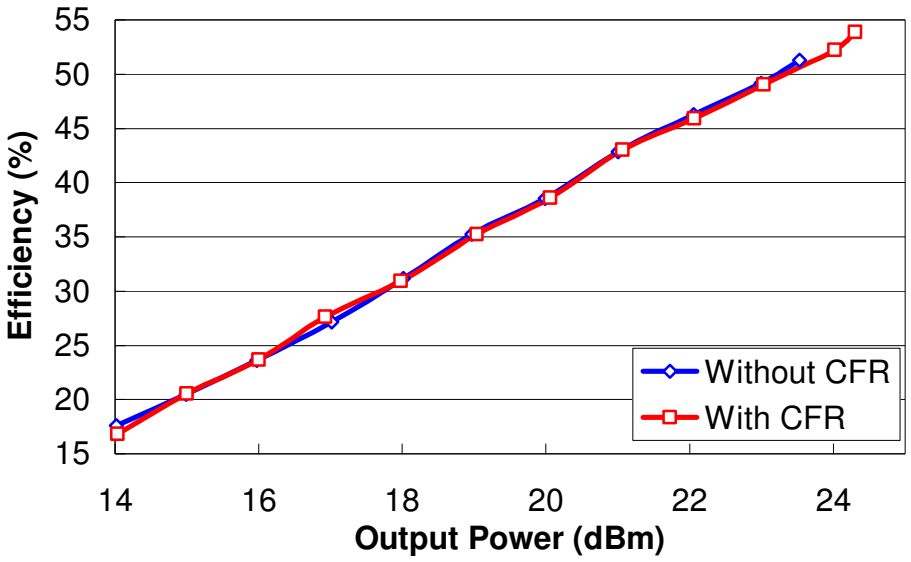


Figure 4.38 Efficiency comparison of EER PA with and without CFR.

Table 4.4 Performance comparison of low-voltage EER PAs

	[43]	[44]	This work w/o CFR	This work with CFR
Modulated Carrier BW	200 kHz	20 MHz	3.84 MHz	3.84 MHz
Supply Voltage	3.3 V	5V	3.5 V	3.5 V
Average Output Power	23.8 dBm	19 dBm	23.5 dBm	24.3 dBm
PAE	22 %	28 %	48.1 %	51.1 %
Gain	25 dB	6.5 dB	12 dB	12.8 dB
Predistortion	Yes	Yes	No	No
Integrated	Yes	No	Partially	Partially

4.7 Dual-Mode PA for Extended Dynamic Range

The dynamic range of an EER PA is limited by the knee voltage of an RF power transistor. For CDMA or W-CDMA applications, the PAs must be able to cover all the output power levels with a dynamic range of up to 80 dB. A dual-mode PA combining both EER and PT technique is proposed. The PA operates in EER mode at high output power levels to attain high peak efficiencies. When backed-off from peak output power, the PA operates in PT mode. While under PT mode, the supply circuit provides a constant DC voltage according to the desired output power level with the gate bias reduced to reduce DC power consumption.

To implement a PT PA, the drain bias of a Sirenza SHF-0289 PA is swept for various power levels to find the suitable bias point. The gate bias voltages and drain bias voltages for various output power levels are shown in Figure 4.39. The PT PA is able to pass the ACLR requirements for W-CDMA from -50 dBm up to 22 dBm output power.

The measured ACLR results are shown in Figure 4.40 and the gain is shown in Figure 4.41. The drain efficiency of the PT PA and the drain efficiency of the EER PA in section 4.4 are compared in Figure 4.42.

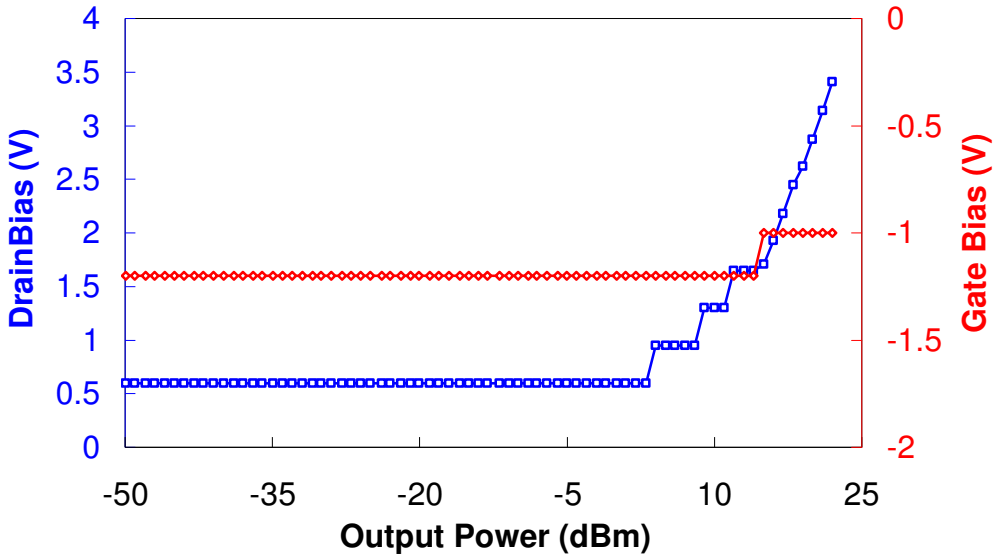


Figure 4.39 Gate bias voltages and drain bias voltages for various output power levels of PT PA.

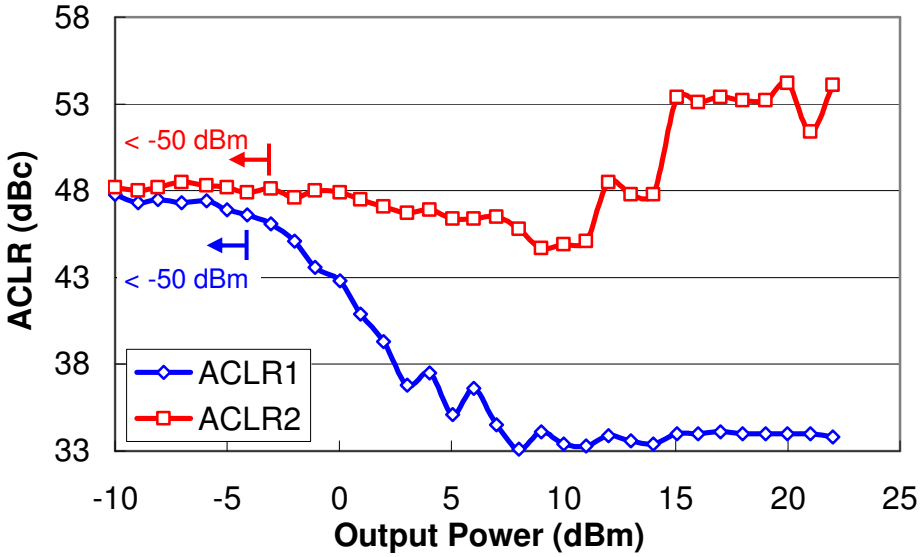


Figure 4.40 Measured ACLR results of PT PA. Results from -50 dBm to -10 dBm do not deviate from the trend shown.

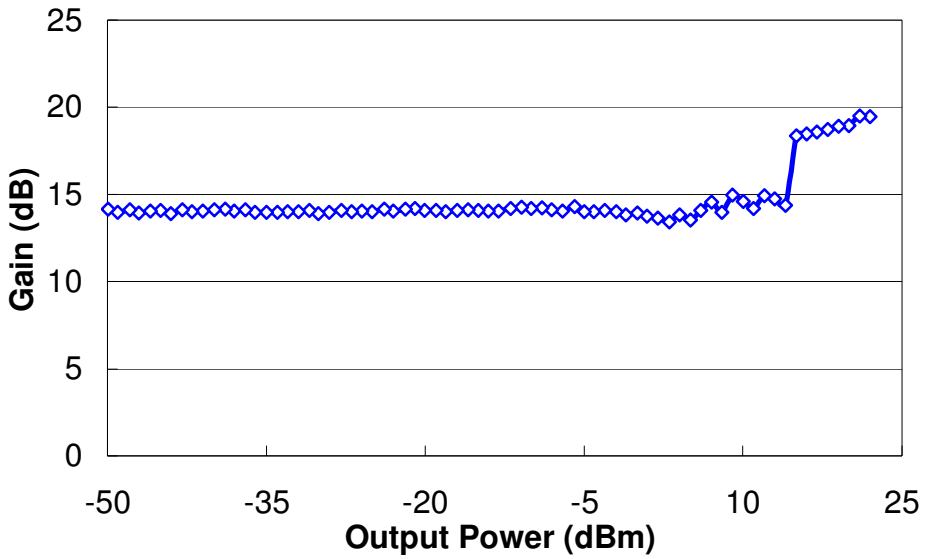


Figure 4.41 Measured gain of PT PA for various output power levels.

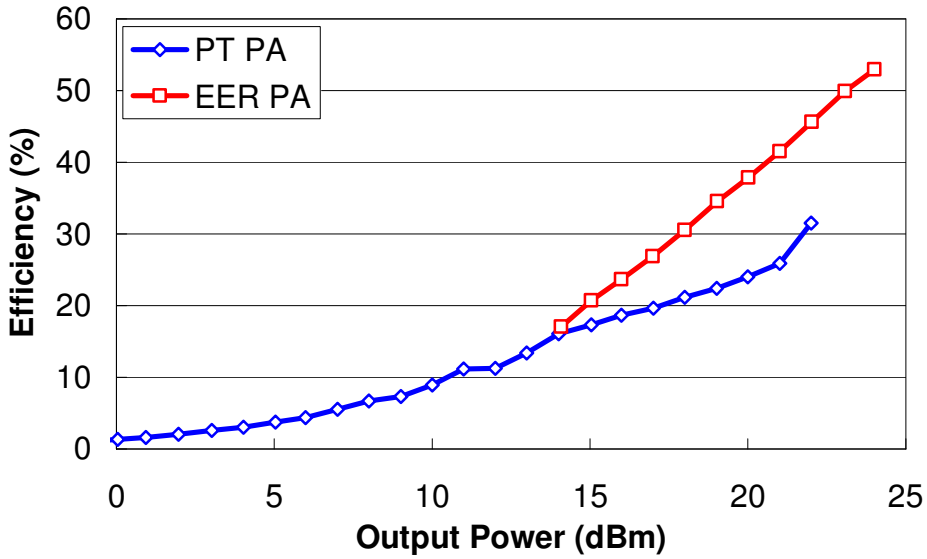


Figure 4.42 Drain efficiency comparison of EER PA and PT PA.

To maximize average efficiency, the dual-mode PA is chosen to operate as an EER PA for output power levels greater than 14 dBm. For power levels less than 14 dBm, the dual-mode PA operates as a PT PA. The drain efficiency and PAE of the dual-mode PA are compared in Figure 4.43. The dual-mode PA is compared with the PT PA and a

commercially available cellular band W-CDMA PA from RF Micro Devices. The RFMD RF5184 is a dual-band dual-stage HBT PA with dynamic biasing of base using mode switching. The output power is normalized to the peak power for comparison and shown in Figure 4.44.

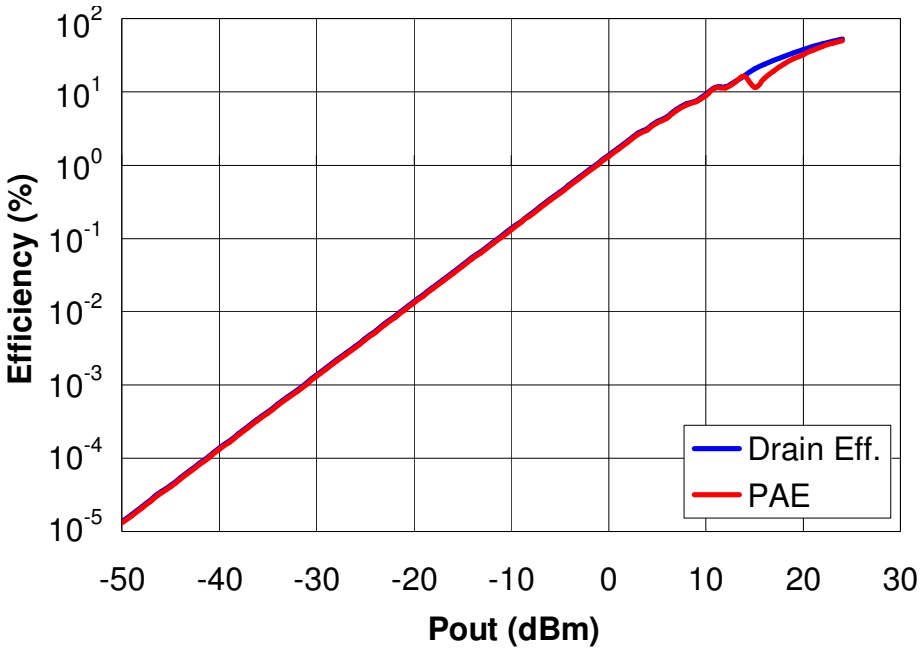


Figure 4.43 Drain efficiency and PAE comparison of dual-mode PA using EER technique for P_{out} greater than 14 dBm and PT technique for lower output power.

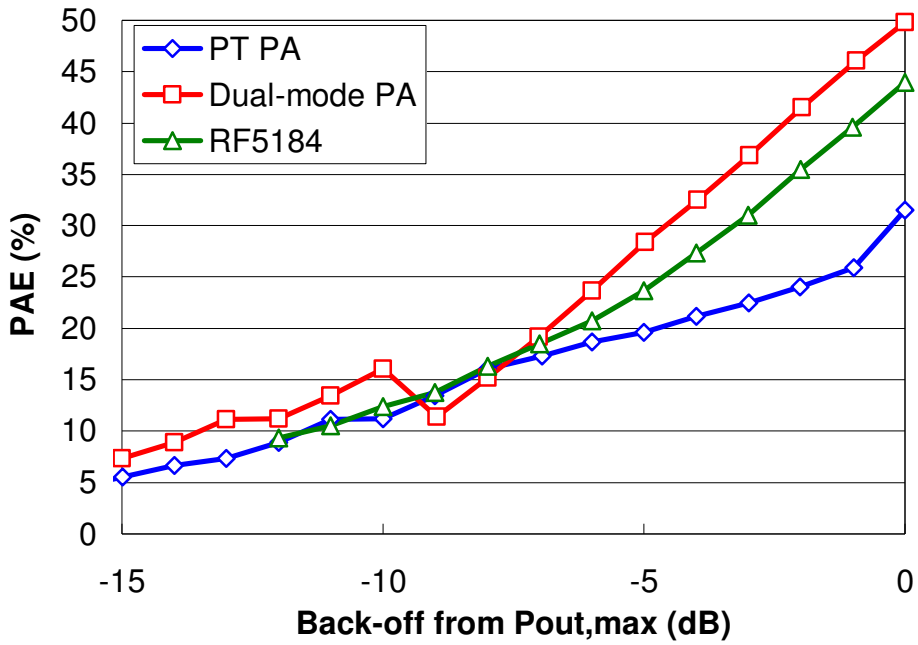


Figure 4.44 PAE comparison of dual-mode PA, PA using only PT technique, and RFMD cellular band W-CDMA PA.

To assess the improvement to battery life, the average efficiency of the dual-mode PA is calculated using (1.3). To calculate the average efficiency, the probability of the output power is required. Recently reported dynamic-biased PAs for W-CDMA applications have all used probability distribution functions for IS-95 CDMA. The works in [4] and [50] use the urban probability distribution function shown in Figure 1.2(a). The work in [47] uses the probability distribution function reported in [22], while the work in [49] uses the IS-95 urban CDMA probability distribution function reported in [4] and [5]. In [46], a probability distribution function for W-CDMA was reported and is shown in Figure 4.45 for a voice-only W-CDMA handheld device with maximum output power of 21 dBm. The average efficiency of the dual-mode PA is calculated using the W-CDMA probability distribution function assuming a combined 3 dB loss in the duplexer and isolator. Average efficiency for the dual-mode PA is also calculated using the probability

distribution function reported in [5] for comparison in Table 4.5 with other recently reported dynamic-biased PAs for W-CDMA applications.

The probability distribution function for W-CDMA reported in [46] is similar to the IS-95 CDMA probability distribution function for suburban areas reported in [5]. Instead of decreasing monotonically at high power levels, the probability distribution function shows a peak close to peak power level. Such peak makes the peak power efficiency an important factor in determining the average of and W-CDMA PA and makes the dual-mode PA in this work attractive.

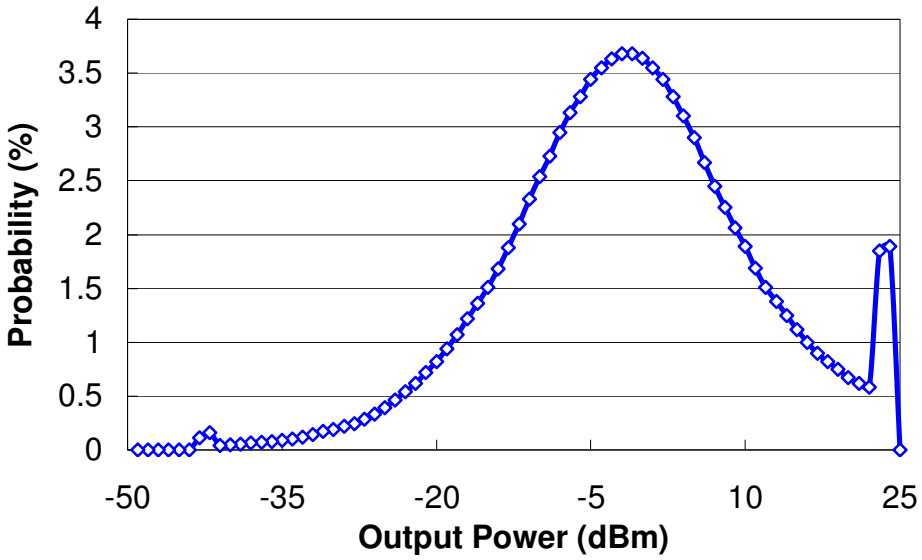


Figure 4.45 W-CDMA probability distribution function reported in [46] normalized to 25 dBm peak output power.

Table 4.5 Efficiency comparison of dynamic-biased PAs for W-CDMA

	Topology	Fixed Biased PA Efficiency	Dynamically Biased PA Efficiency
Noh [4]	Collector Current PT	6.1 %	11.8 %
Fowler [50]	Collector Current PT	2.50 %	4.03 %
Deng [47]	Peripheral Switching	2.50 %	8.08 %
Sahu [49]	Collector Voltage PT	1.95 %	13.67 %
This work (W-CDMA)	Dual-mode EER + PT	-	15.00 %

4.8 Summary

A highly efficient EER-based polar transmitter with a bandwidth sufficient for W-CDMA applications was designed and implemented. Using a 50 MHz dual-phase PWM dynamic supply circuit, a wide bandwidth of supply modulation was achieved without compromising efficiency or spurious output performance. With the use of a digital envelope equalization technique, the linearity of the polar transmitter was improved to pass the stringent ACLR requirements of the W-CDMA standard. Measurement results also show the robustness of this method against supply voltage variations and over a wide range of power levels. Because of the high switching frequency and lower peak current, small-sized 0603 RF inductors and 0402 ceramic capacitors can be used for the off-chip LC filter. With the use of small-sized passives and a small die size of 2.25 mm^2, the

dynamic supply circuit has the potential of being integrated into a PA module to provide a low cost, small-sized, and high efficiency solution for W-CDMA PAs.

Crest factor reduction technique was proposed to be used in conjunction with the polar transmitter. Using CFR with polar transmitters provides increased output power with little added complexity. Performing CFR on polar format signals instead of conventional IQ format signals also reduces system complexity such that the signal need not be converted to polar for CFR and back to IQ format for transmission.

A dual-mode PA combining an EER PA and a PT PA was also proposed. The inherently low dynamic range of an EER PA can be improved by utilizing power-level tracking at low power levels. The low peak power efficiency problem of a PT PA can also be solved by operating as an EER PA at high output power levels. For W-CDMA handheld devices using data services, the peak output power is 24 dBm or higher. To pass the thermal requirement for safe operation, peak power efficiency of over 50% for the PA is required [46]. The proposed dual-mode PA can cover the whole 80 dB dynamic range required by W-CDMA standard while attaining safe operation at peak power

CHAPTER 5

CONCLUSIONS

The objective of the proposed research is to find the suitable dynamic biasing architecture for wideband wireless applications such as W-CDMA. The original contributions include the first development of a dynamic-biased PA using multi-phase supply circuit; the first implementation of a digitally-compensated EER PA for increased efficiency and linearity; the first development of CFR on polar modulated signals; and the first dual-mode PA combining both EER technique and PT technique.

The dynamic biasing technique provides a simple way to improve PA efficiency for applications that require linear amplification. Envelope elimination and restoration (EER) PA or EER-based polar-modulated PA is a highly attractive solution since it has potential to achieve efficiency in excess of 50%. With polar modulation, it is possible to make a multi-mode transmitter with a single RF PA and adapt to environment variation with feedback. In addition, it is possible to remove costly off-chip surface acoustic wave filters and isolators. Without the losses from SAW filters and isolators, the PA transistor size can be reduced and hence reduce overall cost. However, the major drawback is the lack of power-efficient dynamic power supply circuits. To achieve wider bandwidth, an open-loop topology was used, which requires accurate characterization of the RF PA.

First, a dynamic supply circuit using delta modulation was designed and implemented. An open-loop EER PA was constructed and tested with a cellular band IS-95 CDMA signal with bandwidth of 1.25 MHz. It was found by using a low phase

distortion RF PA, the AM-PM performance can be good enough such that the EER PA does not require a RF limiter circuit.

Second, a dynamic supply circuit using dual-phase PWM was designed and implemented to achieve wider bandwidth and higher efficiency. An open-loop EER PA was implemented with the dynamic supply IC. Digital gain compensation was also used to further increase bandwidth and linearity. A cellular band W-CDMA voice signal with 3.84 MHz bandwidth was used to evaluate the performance of the overall PA. To increase the inherent low dynamic range of an EER PA, a dual-mode power amplifier combining an EER PA and power-level tracking PA was developed. With a dual-mode PA, both the peak power efficiency and the efficiency under back-off can be improved so the average efficiency and battery life can be increased. For data services that require safe operation at higher peak power, the proposed dual-mode PA provides a way to produces low enough thermal loss at such power levels, while covering the complete 80 dB dynamic range.

This work will contribute to the development of high efficiency, small-sized multi-mode linear PAs for battery-operated wireless handheld devices.

APPENDIX A

SCHEMATICS OF THE DELTA-MODULATED SUPPLY CIRCUIT

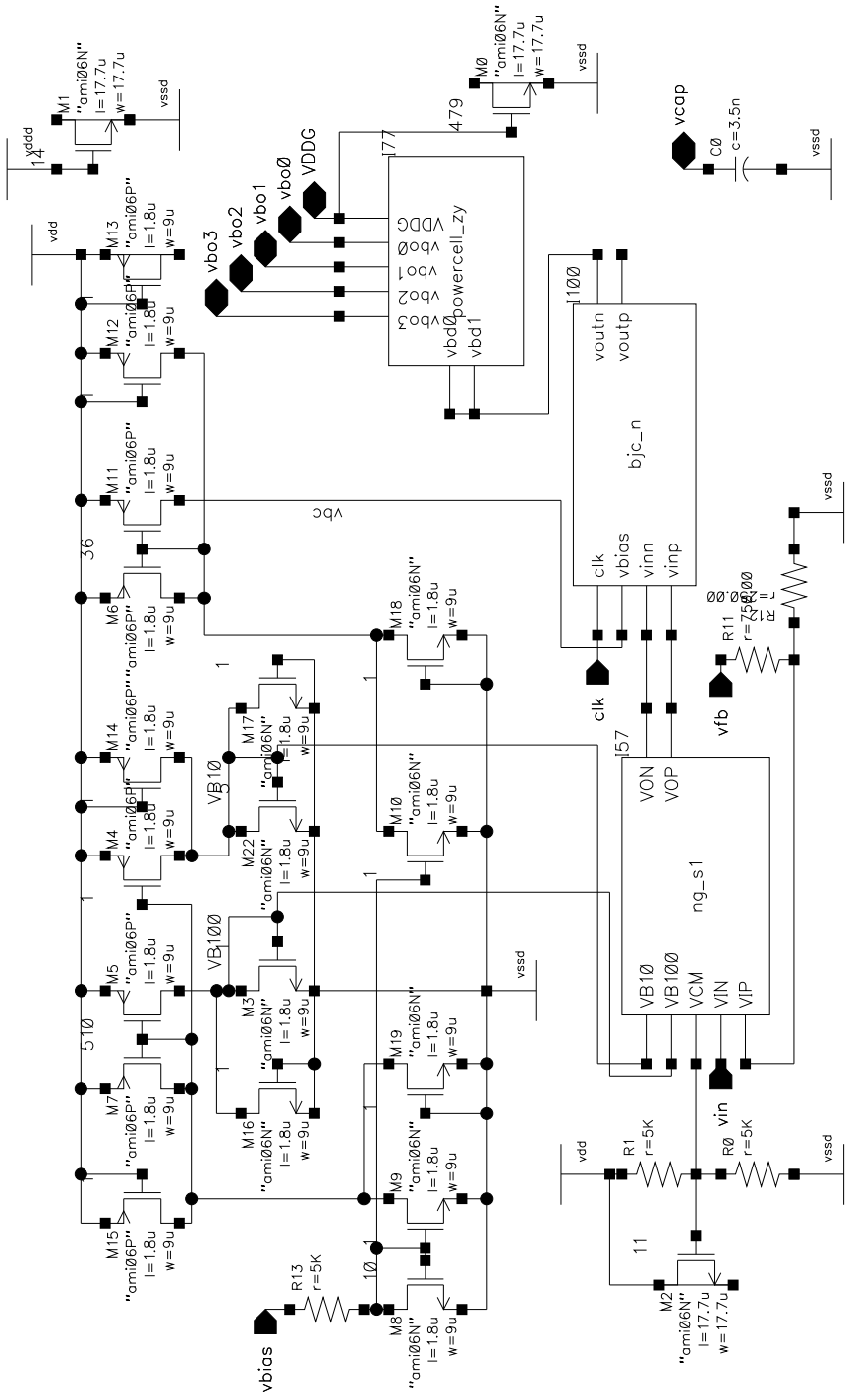


Figure A.1 Schematic of the delta-modulated supply circuit.

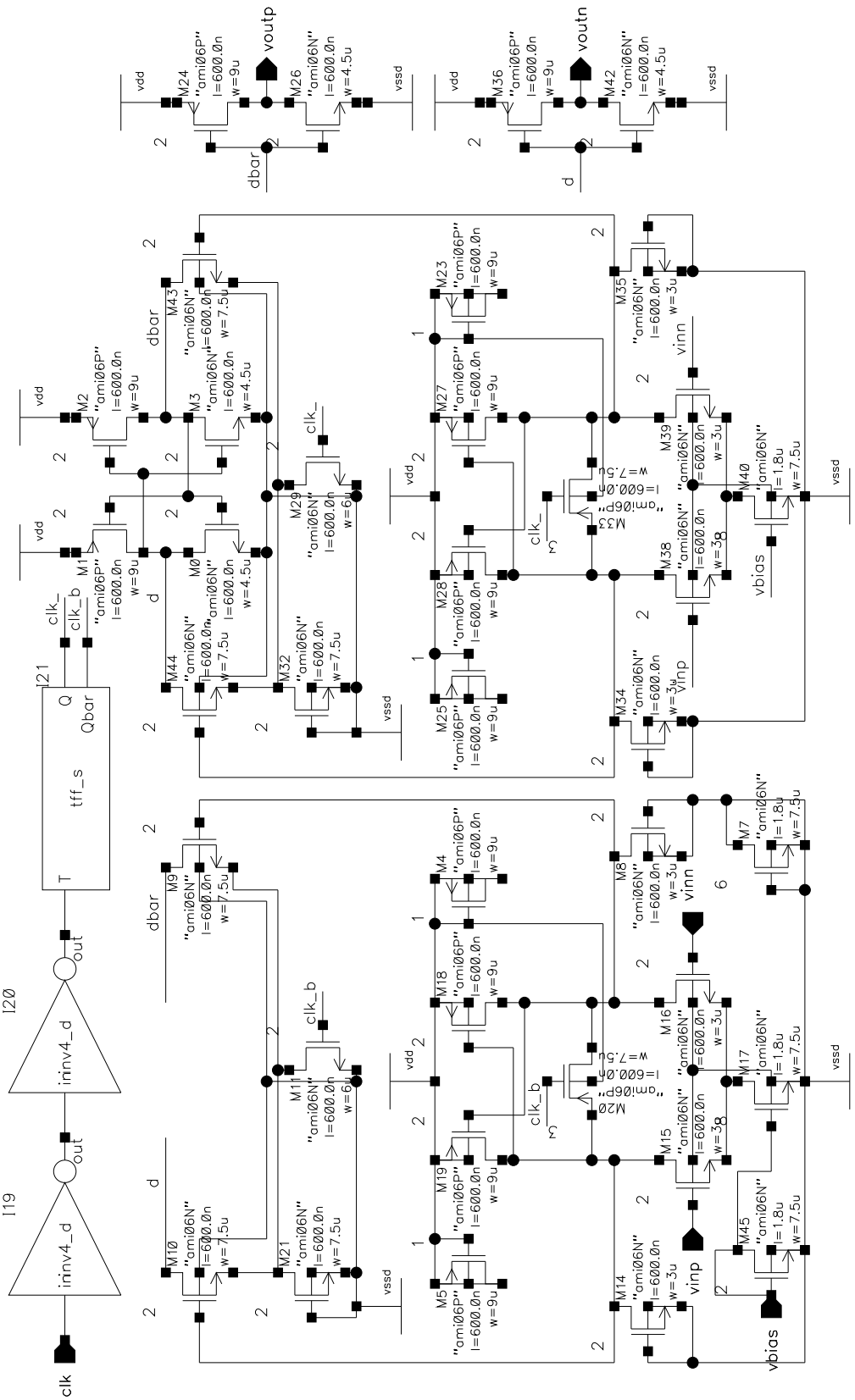


Figure A.2 Schematic of the dual-phase comparator.

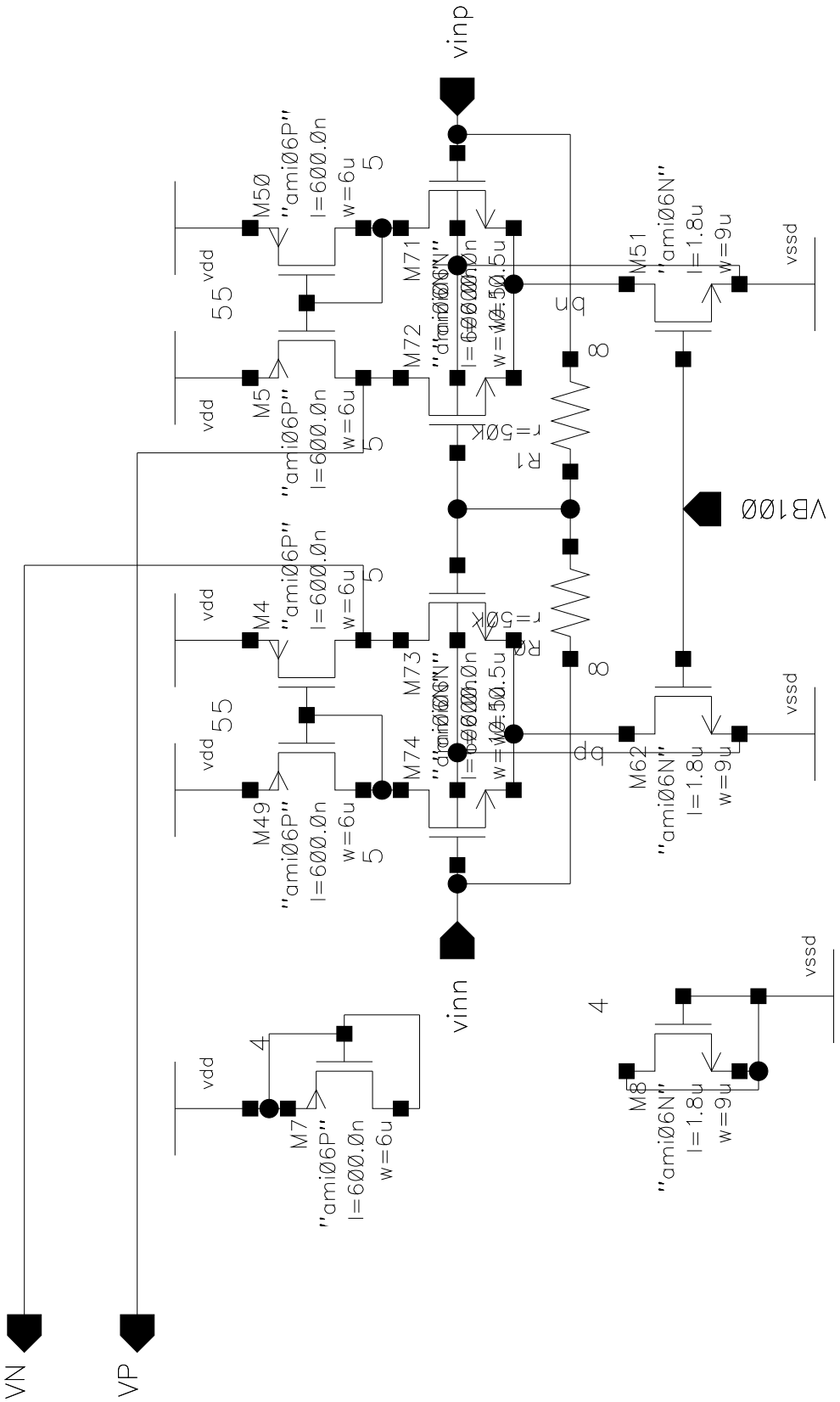


Figure A.3 Schematic of the pre-amplifier.

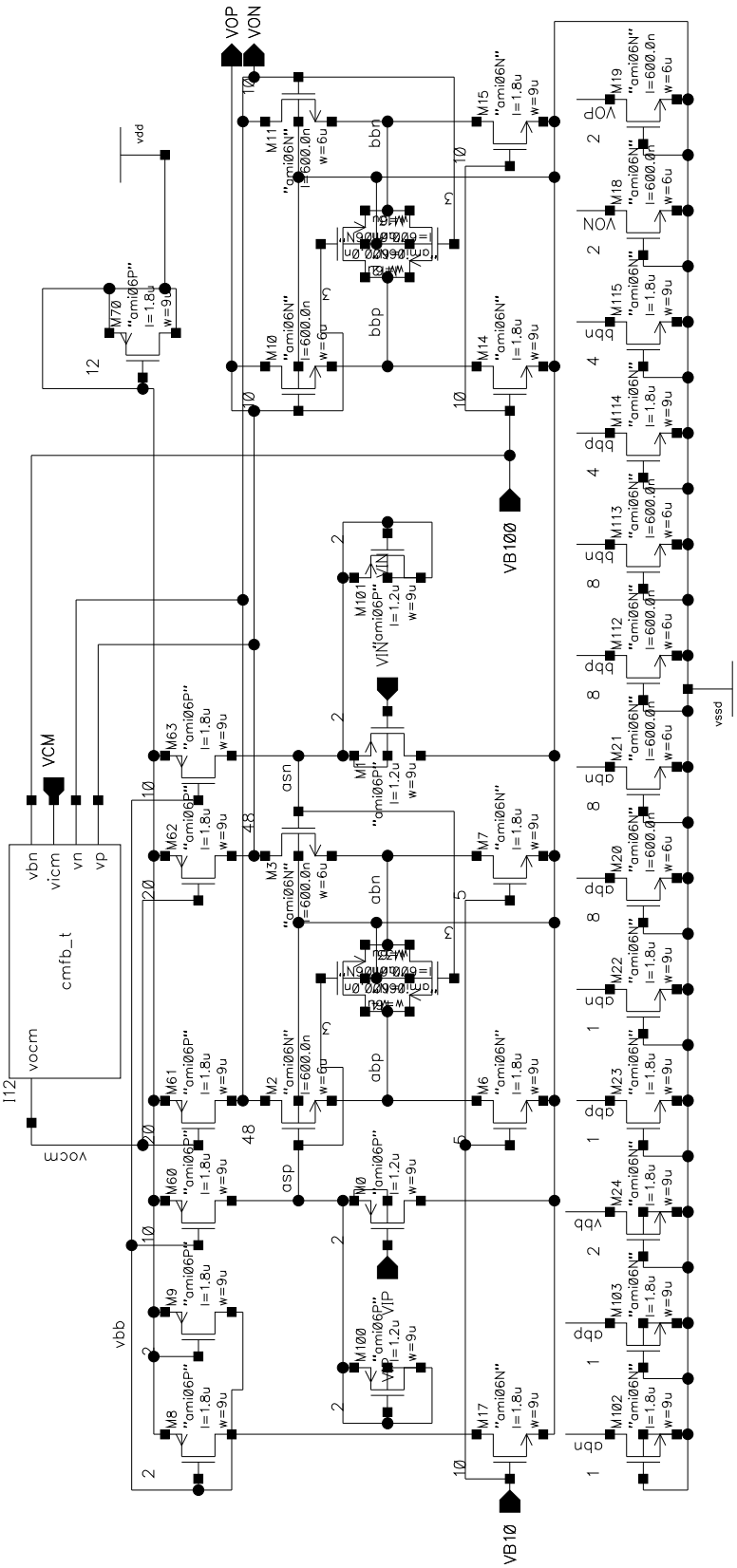


Figure A.4 Schematic of the G_m-C filter for compensation.

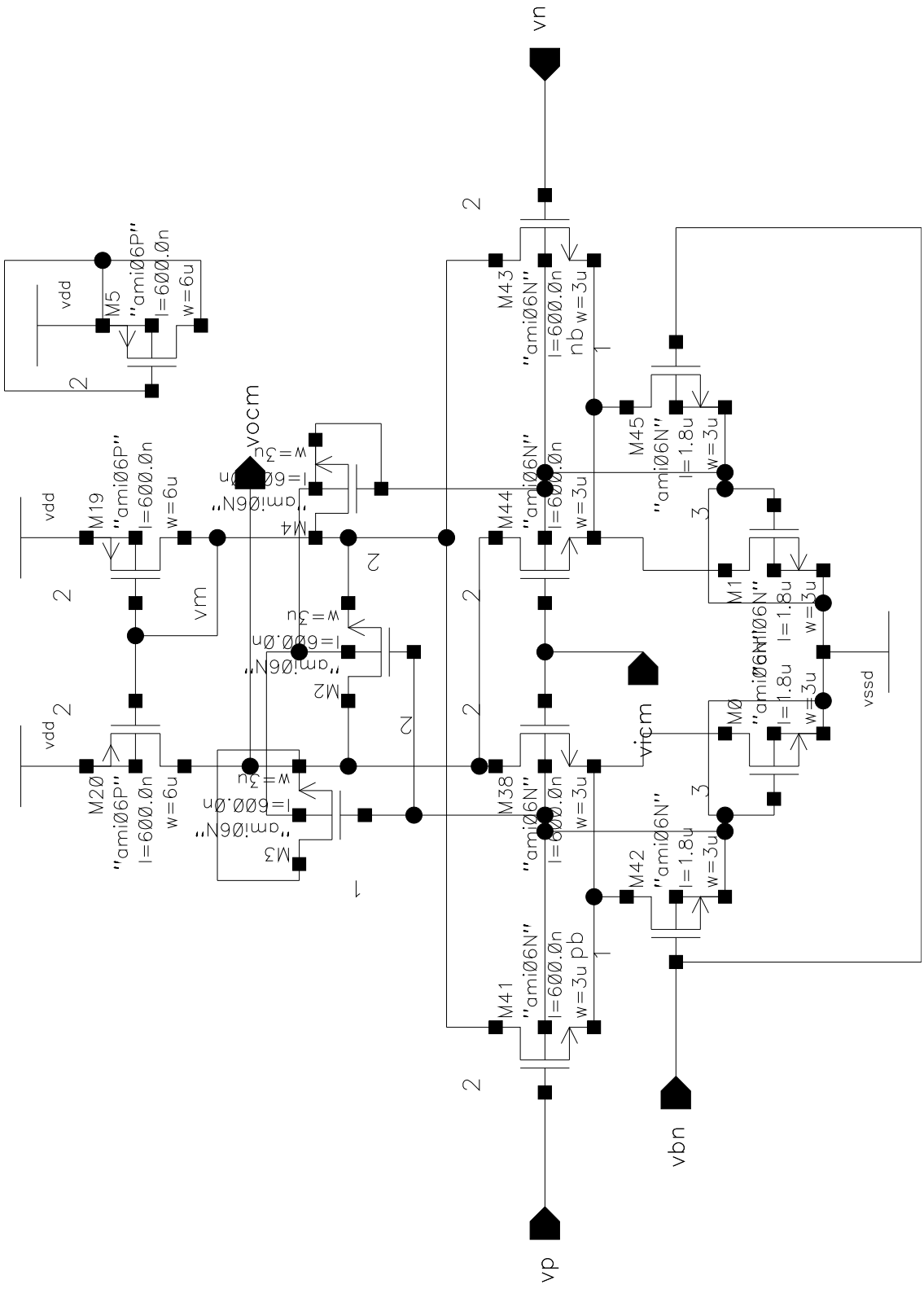


Figure A.5 Schematic of the common-mode feedback circuit for G_m-C filter.

APPENDIX B

SCHEMATICS OF THE DUAL-PHASE PWM SUPPLY CIRCUIT

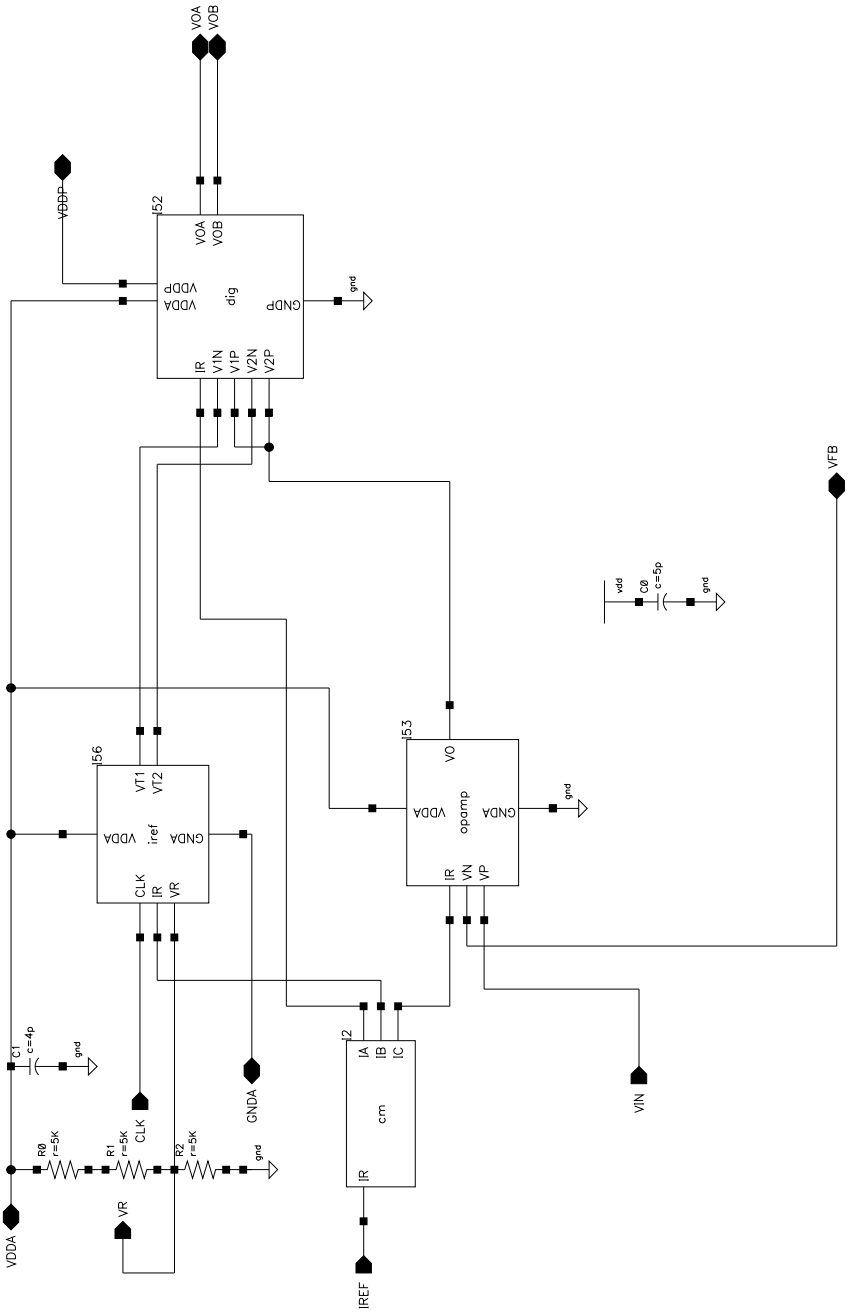


Figure B.1 Schematic of the dual-phase PWM supply circuit.

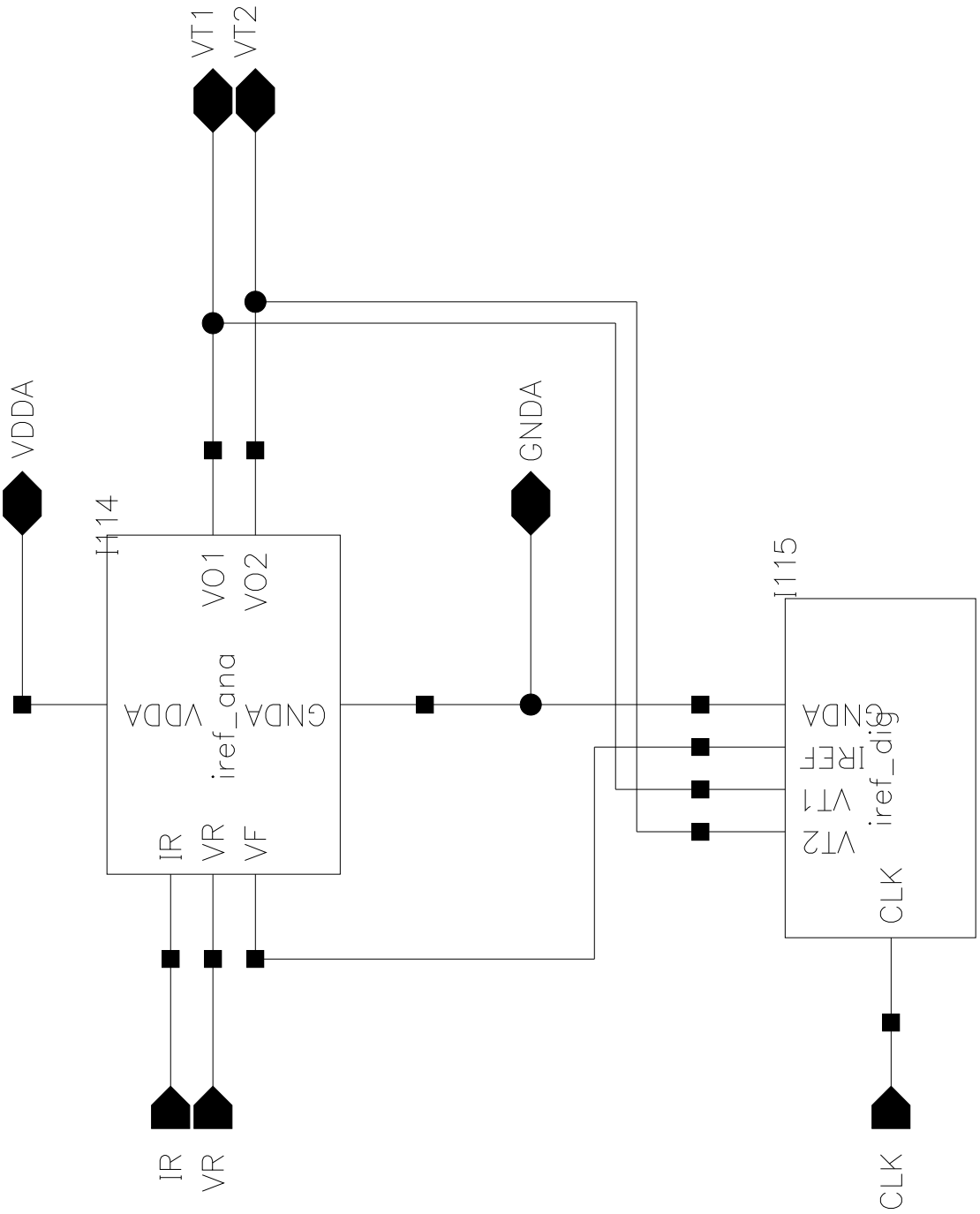


Figure B.2 The sawtooth wave generator.

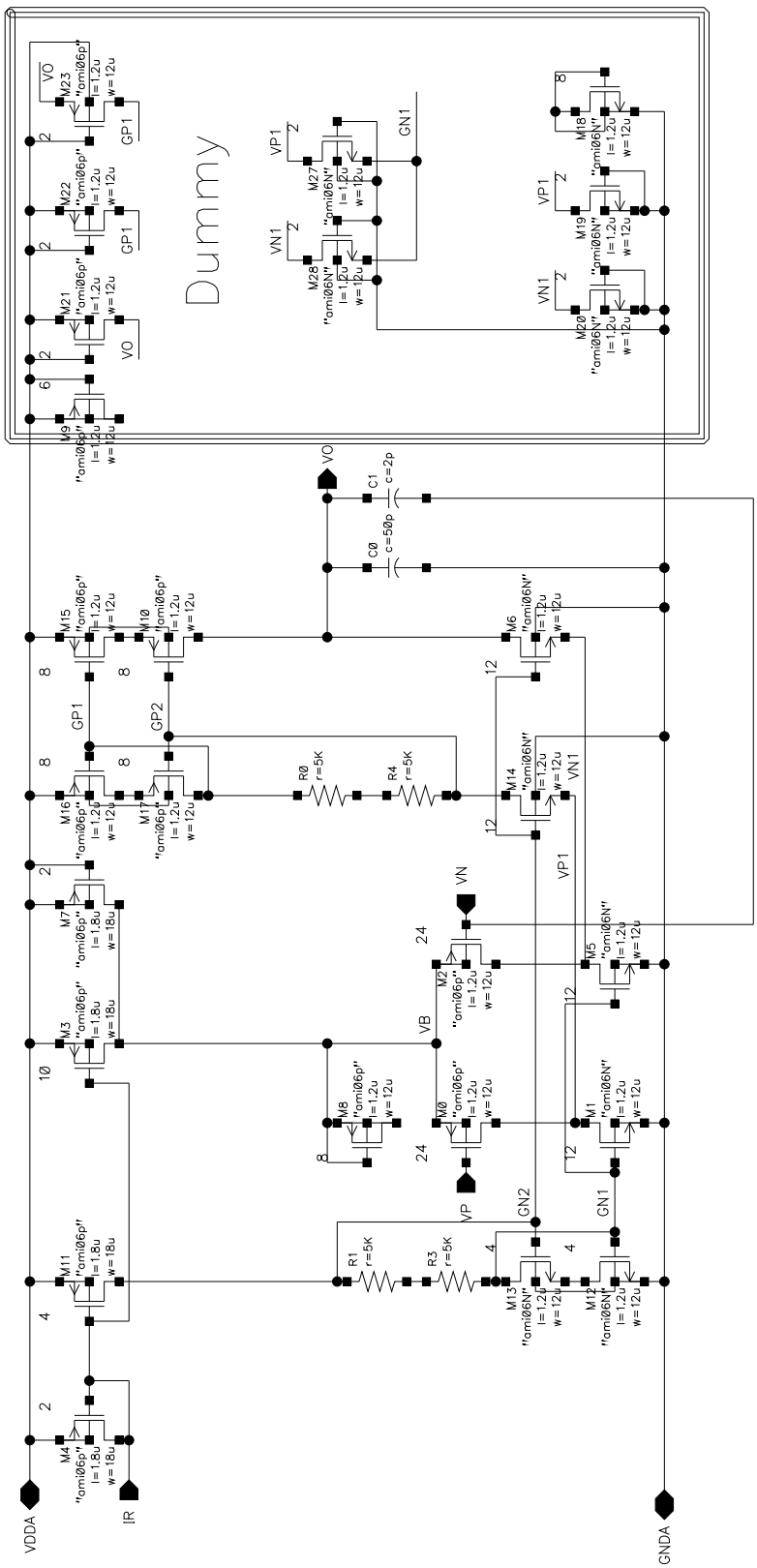


Figure B.3 Schematic of the operational amplifier used for compensation.

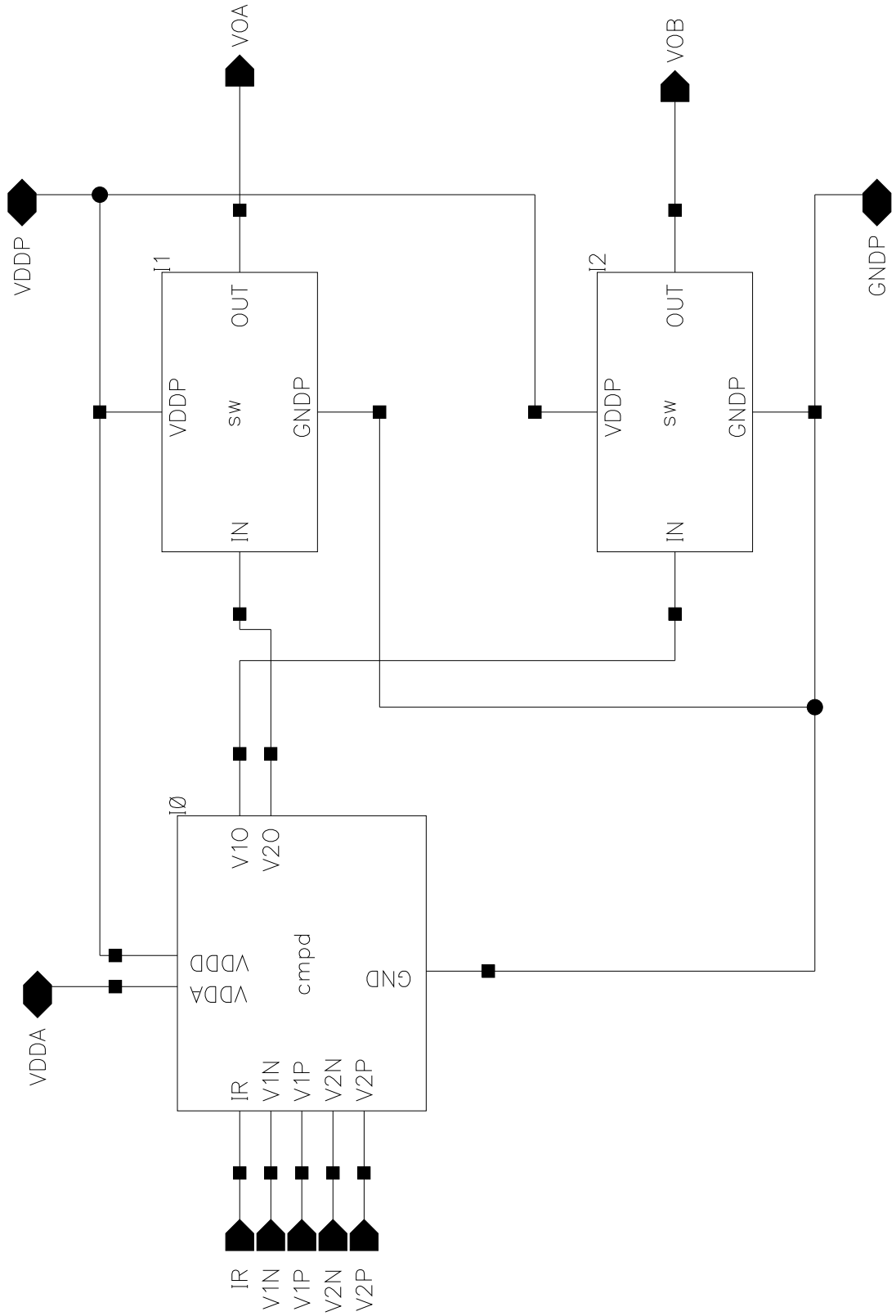


Figure B.4 Schematic of the digital part that includes the comparator and output switches.

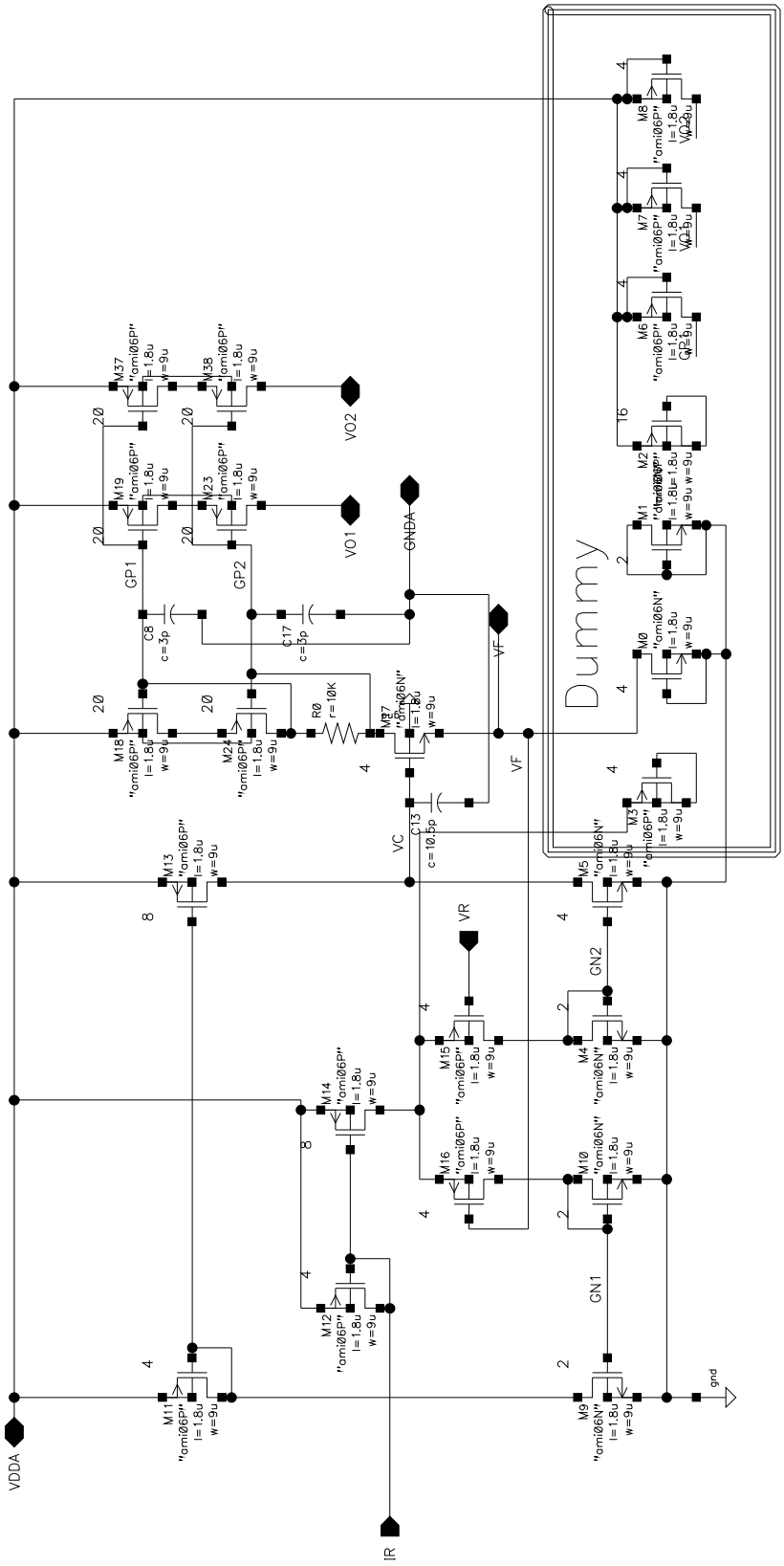


Figure B.5 Schematic of the analog part of the sawtooth generator.

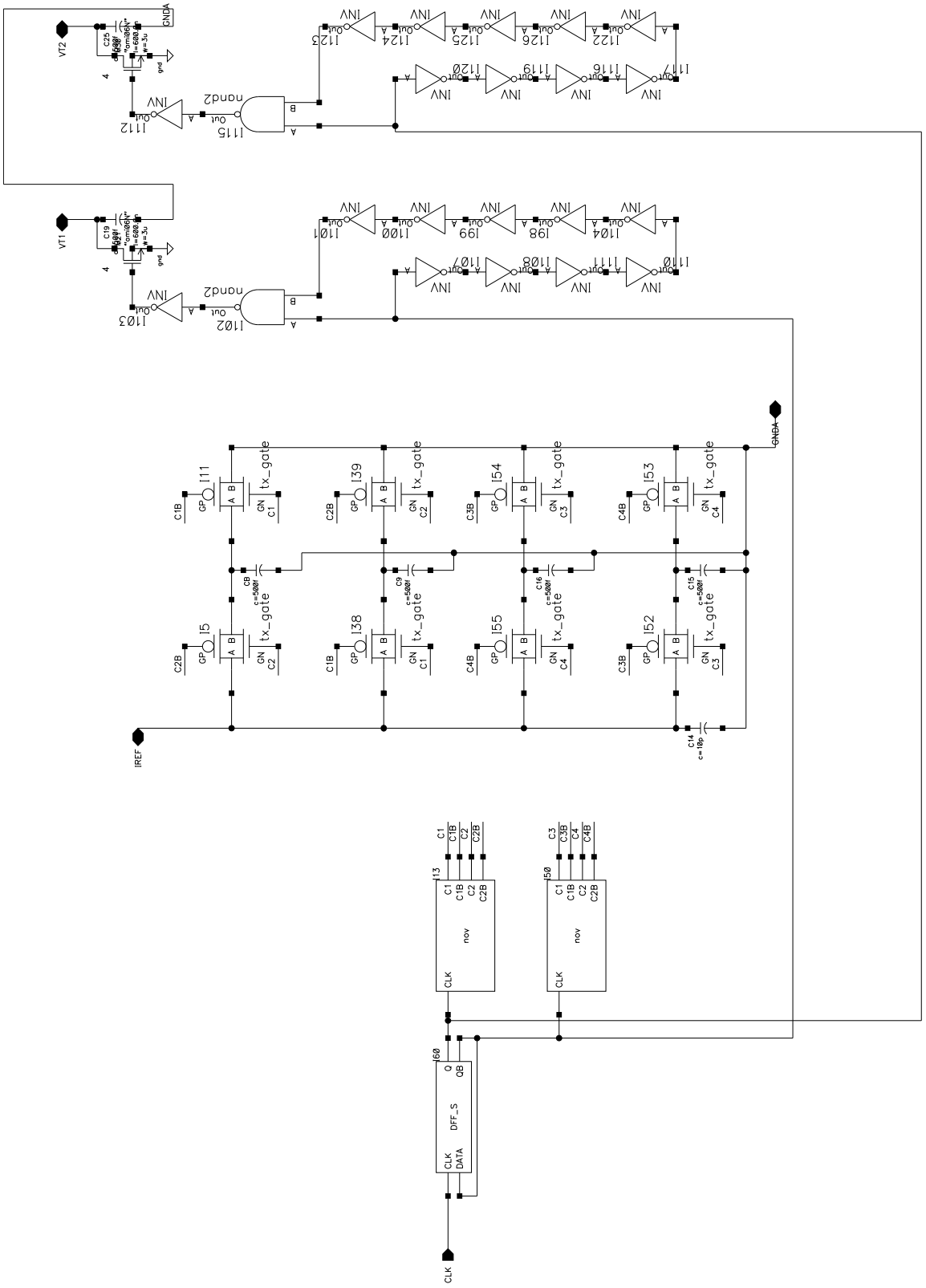


Figure B.6 Schematic of the digital part of the sawtooth generator.

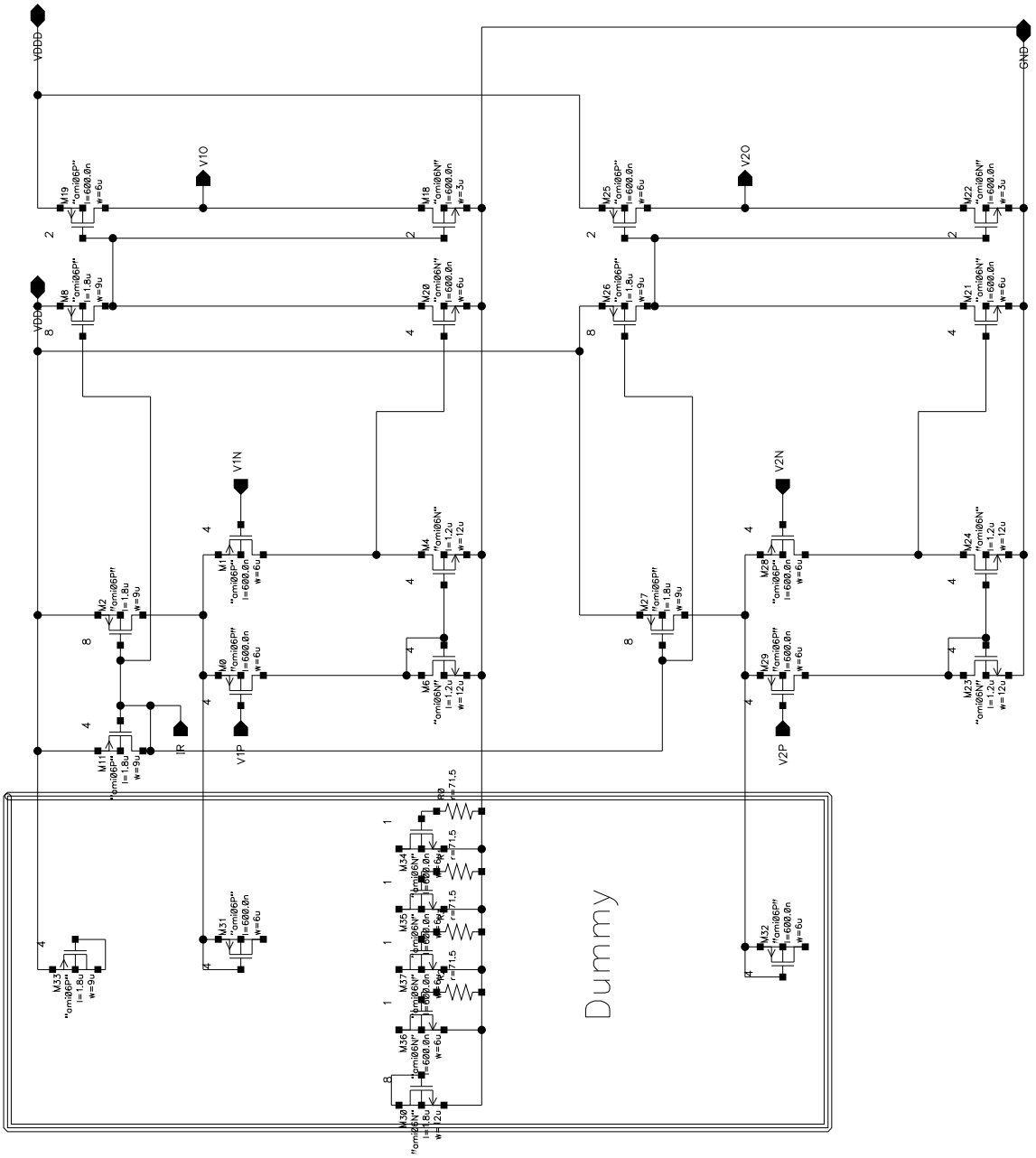


Figure B.7 Schematic of the dual-phase comparator.

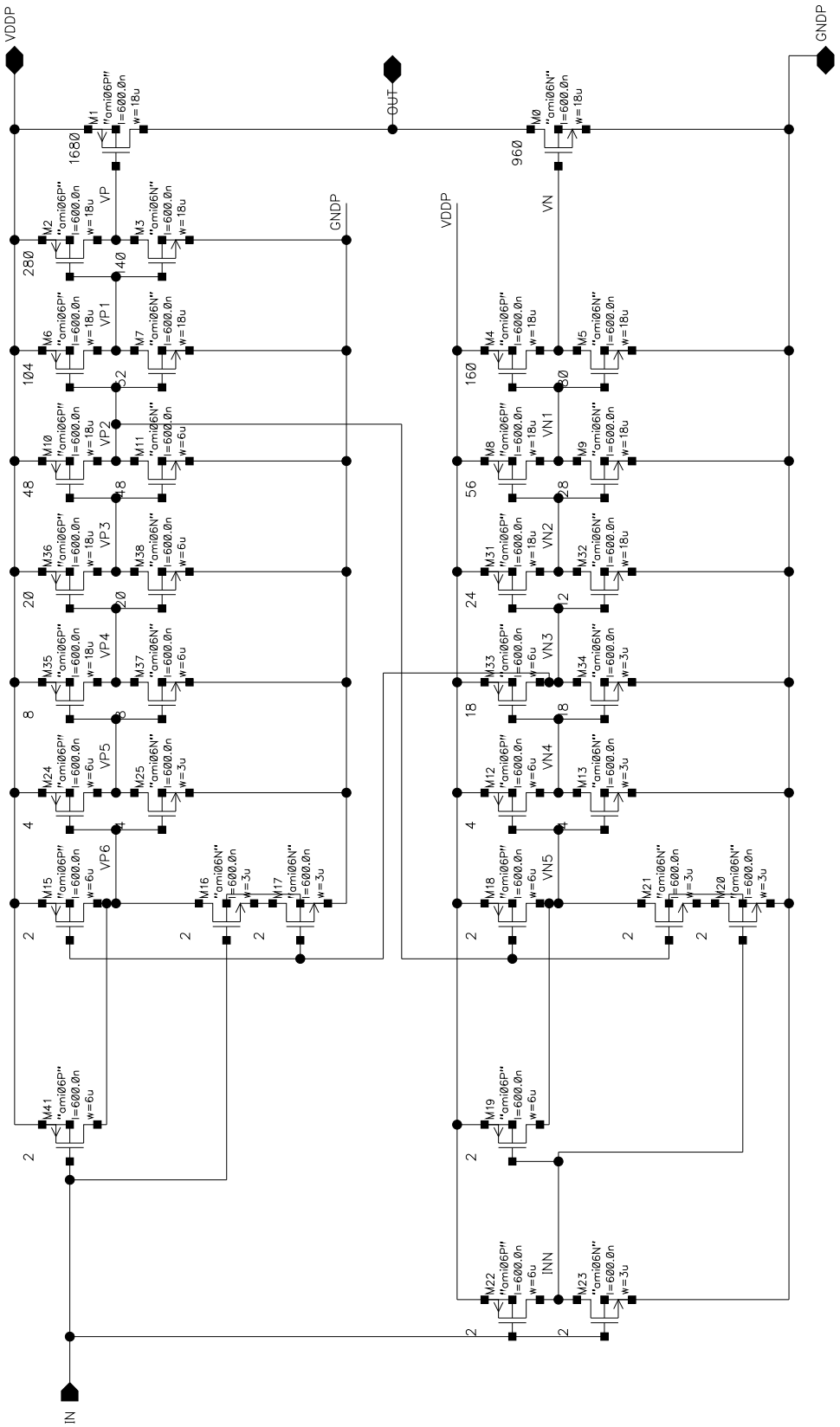


Figure B.8 Schematic of the switch and driver.

REFERENCES

[1] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popovic, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifier and transmitters for RF and microwave," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 3, pp. 814–826, Mar. 2002.

[2] L. R. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proc. IRE*, pp. 803–806, July 1952.

[3] J. B. Groe and L. E. Larson, CDMA Mobile Radio Design. Boston: Artech House, 2000.

[4] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R. Sherman, and T. Quach, "High efficiency CDMA RF power amplifier using dynamic envelope tracking technique," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 873–876, 2000.

[5] B. Sahu and G. A. Rincon-Mora, "A high-efficiency linear RF power amplifier with a power-tracking dynamically adaptive Buck-Boost supply," *IEEE Trans. Microwave Theory Tech.*, vol. 52, no. 1, pp. 112–120, Jan. 2004.

[6] B. Razavi, RF Microelectronics. Prentice Hall, 1998.

[7] E. McCune, "Multi-mode and multi-band polar transmitter for GSM, NADC, and EDGE," *Proc. IEEE Int. Symp. on Circuits and Systems*, 2003.

[8] J. F. Sevic and M. B. Steer, "On the significance of envelope peak-to average ratio for estimating the spectral regrowth of an RF/microwave power amplifier," *IEEE Trans. Microwave Theory Tech.*, vol. 48, no. 6, pp. 1068–1071, June 2000.

[9] F. Wang, A. Ojo, D. Kimball, P. Asbeck, and L. Larson, "Envelope tracking power amplifier with pre-distortion linearization for WLAN 802.11g," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1543 – 1546, 2004.

[10] J. Staudinger, T. Quach, and R. Sherman, "Gate and drain power tracking methods enhance efficiency in reverse link CDMA amplifiers," *Applied Microwave and Wireless Magazine*, pp. 28–38, Mar. 2002.

[11] Y. S. Noh and C. S. Park, "An intelligent power amplifier MMIC using a new adaptive bias control circuit for W-CDMA applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 967–970, June 2004.

[12] N. Srirattana, A. Raghavan, D. Heo, P. Allen, and J. Laskar, "Analysis and design of a high-efficiency multistage Doherty power amplifier for WCDMA," *33rd European Microwave Conference*, vol. 3, pp. 1337–1340, 2003.

[13] M. Iwamoto, A. Williams, P.-F. Chen, A. Metzger, C. Wang, L. Larson, and P. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 931–934, 2001.

[14] Y. Zhao, M. Iwamoto, L. Larson, and P. Asbeck, "Doherty amplifier with DSP control to improve performance in CDMA operation," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 687–690, 2003.

[15] J. Grundlingh, K. Parker, and G. Rabjohn, "A high efficiency Chireix out-phasing power amplifier for 5GHz WLAN applications," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1535–1538, 2004.

[16] F. H. Raab, "High-efficiency single-sideband HF/VHF transmitter based upon envelope elimination and restoration," *HF Radio Systems and Techniques*, pp. 21–25, July 1994.

[17] F. H. Raab, B. E. Sigmon, R. G. Myers, and R. M. Jackson, "L-band transmitter using Kahn EER technique," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 12, pp. 2220–2225, Dec. 1998.

[18] M. J. Koch and R. E. Fisher, "A high efficiency 835 MHz linear power amplifier for digital cellular telephony," *Proc. 39th IEEE Vehicular Tech. Conf.*, pp. 17–18, May 1989.

[19] D. K. Su and W. J. McFarland, "An IC for linearizing RF power amplifiers using envelope elimination and restoration," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2252–2258, Dec. 1998.

[20] D. Rudolph, "Out-of-band emissions of digital transmissions using Kahn EER technique," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 8, pp. 1979–1983, Aug. 2002.

[21] F. H. Raab, "Intermodulation distortion in Kahn technique transmitters," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 12, pp. 2220–2225, Dec. 1996.

[22] G. Hanington, P.-F. Chen, P. M. Asbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Trans. Microwave Theory Tech.*, vol. 47, no. 8, pp. 1471–1476, Aug. 1999.

[23] D. R. Anderson and W. H. Cantrell, "High-efficiency high-level modulator for use in dynamic envelope tracking CDMA RF power amplifiers," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1509–1512, 2001.

[24] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R. Sherman, T. Quach, and V. Wang, "800 MHz power amplifier using envelope following technique," *Proc. IEEE Radio and Wireless Conf.*, pp. 301–304, Aug. 1999.

[25] T. Sowlati, D. Rozenblit, R. Pullela, M. Damgaard, E. McCarthy, D. Koh, D. Ripley, F. Balteanu, and I. Gheorghe, "Quad-band GSM/GPRS/EDGE polar loop transmitter," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2179–2189, Dec. 2004.

[26] A. Hadjichristos, "Transmit architectures and power control schemes for low cost highly integrated transceivers for GSM/EDGE applications," *Proc. Custom Integrated Circuits Conf.*, vol. 3, pp. 610–613, 2003.

[27] A. Hadjichristos, J. Walukas, N. Klemmer, W. Suter, S. Justice, S. Uppathil, and G. Scott, "A highly integrated quad band low EVM polar modulation transmitter for GSM/EDGE applications," *Proc. Custom Integrated Circuits Conf.*, pp. 565–568, 2004.

[28] M. Elliott, T. Montalvo, B. Jeffries, F. Murden, J. Strange, A. Hill, S. Nandipaku, and J. Harrebek, "A polar modulator transmitter for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2190–2199, Dec. 2004.

[29] J. Staudinger, "Applying switched gain stage concepts to improve efficiency and linearity for mobile CDMA power amplification," *Microwave J.*, vol. 43, no. 9, pp. 152–162, Sep. 2000.

[30] S. Kim, J. Lee, J. Shin, and B. Kim, "CDMA handset power amplifier with a switched output matching circuit for low/high power mode operations," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1523–1526, 2004.

[31] Y.-J. Jeon, H.-W. Kim, H.-T. Kim, G.-H. Ryu, J.-Y. Choi, K. Kim, S.-E. Sung, and B. O, "A highly efficient CDMA power amplifier based on parallel amplification architecture," *IEEE Microwave Wireless Compon. Lett.*, vol. 14, no. 9, pp. 401–403, Sep. 2004.

[32] P. Nagle, P. Burton, E. Heaney, and F. McGrath, "A wide-band linear amplitude modulator for polar transmitters based on the concept of interleaving delta modulation," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1748–1756, Dec. 2002.

[33] N. Schlumpf, M. Declercq, and C. Dehollain, "A fast modulator for dynamic supply linear RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1015–1025, July 2004.

[34] D. Pehlke, A. Hadjichristos, and S. Justice, "High performance open-loop AM modulator designed for power control of E-GPRS polar modulated power amplifier," *Proc. Custom Integrated Circuits Conf.*, pp. 569–572, 2004.

[35] J.-H. Chen, K. U-yen, and J. S. Kenney, "An envelope elimination and restoration power amplifier using a CMOS dynamic power supply circuit," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 3, pp. 1519–1522, 2004.

[36] S. Haykin, *Communication Systems*, 4th ed. New York: John Wiley & Son, 2001.

[37] G. M. Blair, "Comments on new single-clock CMOS latches and flip-flops with improved speed and power savings," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1610–1611, Oct. 1997.

[38] HPSK for 3G, Agilent Application Note AN1335, 2000.

[39] P. Hazucha, *et. al.,* "A 233MHz, 80-87% efficient, integrated, 4-phase DC-DC converter in 90nm CMOS," *Symp. on VLSI Circuits Dig. Tech. Papers*, pp. 256-57, 2004.

[40] R. Sperlich, Y. Park, G. Copeland, and J. S. Kenney, "Power amplifier linearization with digital predistortion and crest factor reduction," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol. 2, pp. 669–672, 2004.

[41] N. Chen and G.T. Zhou, "Distortionless crest factor reduction for forward link CDMA," *IEEE Workshop on Signal Processing Advances in Wireless Comm.*, pp. 294–297.

[42] K. Yadavelli, D. Efstathiou, and M. Manglani, " Crest factor reduction engine for multi-carrier WCDMA transmitted signals," *IEEE Int. Symp. on Personal, Indoor and Mobile Radio Comm.*, vol. 3, pp. 2207–2211, 2005.

[43] P. Reynaert and M. S. J. Steyaert, "A 1.75-GHz polar modulated CMOS RF power amplifier for GSM-EDGE," *IEEE J. Solid-State Circuits*, vol. 40, pp. 2598–2608, Dec. 2005.

[44] F. Wang, D. Kimball, J. Popp, A. Yang, D. Lie, P. Asbeck, and L. Larson, "Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications," *IEEE MTT-S Int. Microwave Symp. Digest*, vol. 2, pp. 645–648, 2005.

[45] Ube Electronics UX0836L157 data sheet, 2005.

[46] H. Lilja and H. Mattila, "WCDMA power amplifier requirements and efficeincy optimization criteria," *IEEE MTT-S Int. Microwave Symp. Digest*, vol. 3, pp. 1843–1846, 1999.

[47] J. Deng, P. S. Gudem, L. E. Larson, and P. M. Asbeck, "A high average-efficiency SiGe HBT power amplifier for WCDMA handset applications," *IEEE Trans. Microwave Theorey Tech.*, vol. 53, no. 2, pp. 529-537, Feb. 2005.

[48] H. Lilja and H. Mattila, "WCDMA uplink modulation scheme evolution and transmitter implementation," *IEEE Vehicular Tech. Conf. Digest*, pp. 899–903, 1999.

[49] B. Sahu, "Integrated, dynamically adaptive supplies for linear RF power amplifiers in portable applications," *Georgia Institute of Technology Ph.D. Dissertation*, May 2005.

[50] T. Fowler, K. Burger, N.-S. Cheng, A. Samelis, E. Enobakhare, and S. Rohlfing, "Efficeincy improvement techniques at low poer levels for linear CDMA and WCDMA power amplifiers," *IEEE RFIC Symp. Dig.*, pp. 41-44, June 2002.

[51] P. M. Asbeck, L. E. Larson, and I. G. Galton, "Synergistic design of DSP and power amplifiers for wireless communications," *IEEE Trans. Microwave Theorey and Tech.*, vol. 49, no. 11, pp. 2163-2169, Nov. 2001.

[52] S. C. Cripps, Advanced Techniques in RF Power Amplifier Design. Artech House, 2002.

[53] J.-H. Chen, P. Fedorenko, and J. S. Kenney, "A low-voltage polar transmitter with digital envelope path gain compensation," IEEE Microwave and Wireless Component Letters, Jul. 2006.